FEATURES

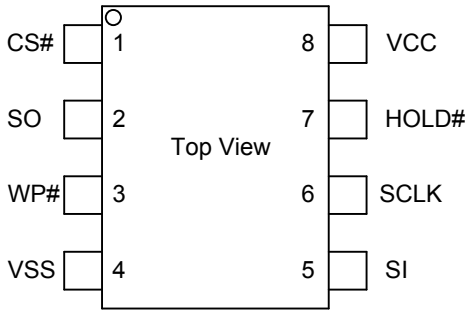
- 4M/2M/1M/512K-bit Serial Flash
  - -512/256/128/64K-byte
  - -256 bytes per programmable page
- Standard, Dual, Quad SPI
  - -Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - -Dual SPI:SCLK, CS#, IO0, IO1, WP#, HOLD#
  - -Quad SPI:SCLK, CS#, IO0, IO1, IO2, IO3
- High Speed Clock Frequency
  - -120MHz for fast read with 30PF load
  - -Dual I/O Data transfer up to 240Mbits/s
  - -Quad I/O Data transfer up to 480Mbits/s
- Software/Hardware Write Protection
  - -Write protect all/portion of memory via software
  - -Enable/Disable protection with WP# Pin
  - -Top or Bottom, Sector or Block selection
- Minimum 100,000 Program/Erase Cycles
- Program/Erase Speed
  - -Page Program time:0.7ms typical
  - -Sector Erase time:150ms typical
  - -Block Erase time:0.3\0.5s typical
  - -Chip Erase time:3\2\1\0.5s typical
- Flexible Architecture
  - -Sector of 4K-byte
  - -Block of 32/64K-byte
- Low Power Consumption
  - -20mA maximum active current
  - -5uA maximum power down current
- Advanced security Features(1)
  - -16-Bit Customer ID
  - -Security Architecture
- Single Power Supply Voltage
  - -Full voltage range:2.7~3.6V

Note: 1.Please contact Gigadevice for details.

GENERAL DESCRIPTION

The GD25Q40/20/10/512 (4M-bit) SPI flash supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). SPI clock frequencies of up to 120MHz are supported allowing equivalent clock rates of 240MHz for Dual Output & Dual I/O read command, and 480MHz for Quad output & Quad I/O read command.

CONNECTION DIAGRAM

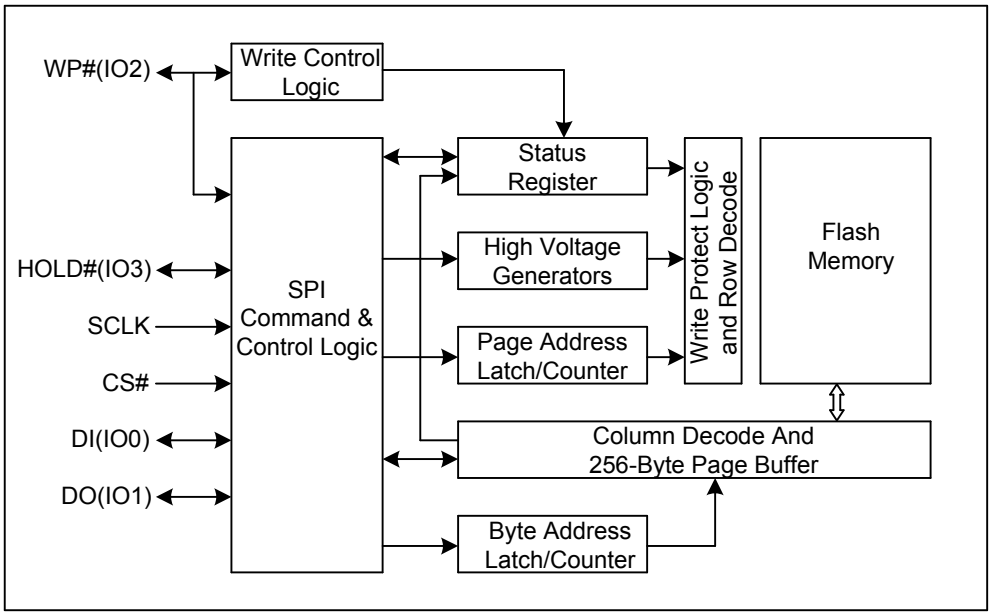


8 – LEAD SOP/DIP

PIN DESCRIPTION

Pin Name	I/O	Description
CS#	**I**	Chip Select Input
SO (IO1)	**I/O**	Data Output (Data Input Output 1)
WP# (IO2)	**I/O**	Write Protect Input (Data Input Output 2)
VSS		Ground
SI (IO0)	**I/O**	Data Input (Data Input Output 0)
SCLK	**I**	Serial Clock Input
HOLD# (IO3)	**I/O**	Hold Input (Data Input Output 3)
VCC		Power Supply

BLOCK DIAGRAM



MEMORY ORGANIZATION

GD25Q40

Each device has	Each block has	Each sector has	Each page has	
512K	64/32K	4K	256	bytes
2K	256/128	16	-	pages
128	16/8	-	-	sectors
8/16	-	-	-	blocks

GD25Q20

Each device has	Each block has	Each sector has	Each page has	
256K	64/32K	4K	256	bytes
1K	256/128	16	-	pages
64	16/8	-	-	sectors
4/8	-	-	-	blocks

GD25Q10

Each device has	Each block has	Each sector has	Each page has	
128K	64/32K	4K	256	bytes
512	256/128	16	-	pages
32	16/8	-	-	sectors
2/4	-	-	-	blocks

GD25Q512

Each device has	Each block has	Each sector has	Each page has	
64K	32K	4K	256	bytes
256	128	16	-	pages
16	8	-	-	sectors
2	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25Q40 64K Bytes Block Sector Architecture

Block	Sector	Address range	
7	127	07F000H	07FFFFH
	……	……	……
	112	070000H	070FFFH
6	111	06F000H	06FFFFH
	……	……	……
	96	060000H	060FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

GD25Q20 64K Bytes Block Sector Architecture

Block	Sector	Address range	
3	64	03F000H	03FFFFH
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

GD25Q10 64K Bytes Block Sector Architecture

Block	Sector	Address range	
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

GD25Q512 32K Bytes Block Sector Architecture

Block	Sector	Address range	
1	15	00F000H	00FFFFH
	……	……	……
	8	008000H	008FFFH
0	7	007000H	007FFFH
	……	……	……
	0	000000H	000FFFH

DEVICE OPERATION

SPI Mode

Standard SPI

The GD25Q40/20/10/512 feature a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25Q40/20/10/512 supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The GD25Q40/20/10/512 supports Quad SPI operation when using the “Quad Output Fast Read”,” Quad I/O Fast Read”, “Quad I/O Word Fast Read” (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

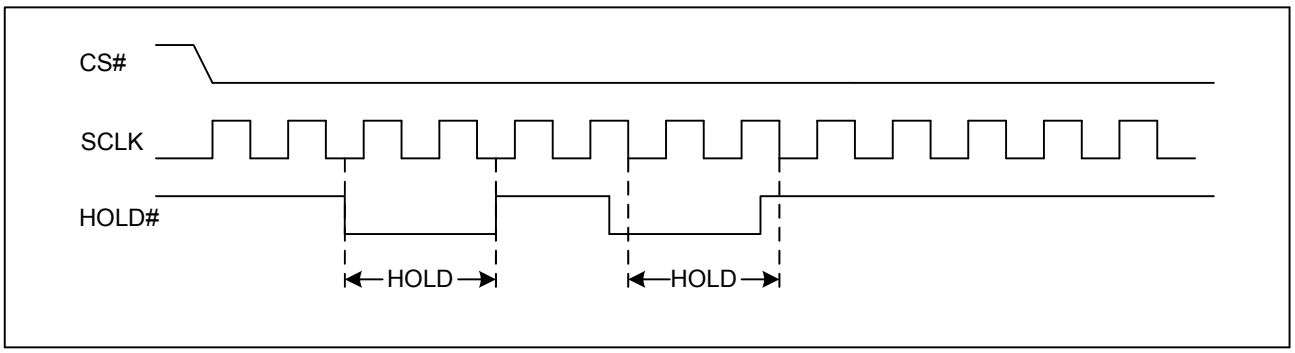
Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure1. Hold Condition



Data Protection

The GD25Q40/20/10/512 provides the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Sector Erase (SE)
  -Block Erase (BE)
  -Chip Erase (CE)
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# going low to protected the BP0~BP4 bits and SRP0~1 bits.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

Table1.0. GD25Q40 Protected area size

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	7	070000H-07FFFFH	64KB	Upper 1/8
0	0	0	1	0	6 and 7	060000H-07FFFFH	128KB	Upper 1/4
0	0	0	1	1	4 to 7	040000H-07FFFFH	256KB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/8
0	1	0	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/4
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/2
0	X	1	X	X	0 to 7	000000H-07FFFFH	512KB	ALL
1	0	0	0	1	7	07F000H-07FFFFH	4KB	Top Block
1	0	0	1	0	7	07E000H-07FFFFH	8KB	Top Block
1	0	0	1	1	7	07C000H-07FFFFH	16KB	Top Block
1	0	1	0	X	7	078000H-07FFFFH	32KB	Top Block
1	0	1	1	0	7	078000H-07FFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block
1	X	1	1	1	0 to 7	000000H-07FFFFH	512KB	ALL

Table1.1. GD25Q20 Protected area size

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	X	X	0	0	NONE	NONE	NONE	NONE
0	0	X	0	1	3	030000H – 03FFFFH	64KB	Upper 1/4
0	0	X	1	0	2 and 3	020000H – 03FFFFH	128KB	Upper 1/2
0	1	X	0	1	0	000000H – 00FFFFH	64KB	Lower 1/4
0	1	X	1	0	0 and 1	000000H – 01FFFFH	128KB	Lower 1/2
0	X	X	1	1	0 to 3	000000H – 03FFFFH	256KB	ALL
1	X	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	3	03F000H-03FFFFH	4KB	Top Block
1	0	0	1	0	3	03E000H-03FFFFH	8KB	Top Block
1	0	0	1	1	3	03C000H-03FFFFH	16KB	Top Block
1	0	1	0	X	3	038000H-03FFFFH	32KB	Top Block
1	0	1	1	0	3	038000H-03FFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block
1	X	1	1	1	0 to 3	000000H-03FFFFH	256KB	ALL

Table1.2. GD25Q10 Protected area size

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	X	X	0	0	NONE	NONE	NONE	NONE
0	0	X	0	1	1	010000H-01FFFFH	64KB	Upper 1/2
0	1	X	0	1	0	000000H-00FFFFH	64KB	Lower 1/2
0	X	X	1	X	0 to 1	000000H-01FFFFH	128KB	ALL
1	X	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	1	01F000H-01FFFFH	4KB	Top Block
1	0	0	1	0	1	01E000H-01FFFFH	8KB	Top Block
1	0	0	1	1	1	01C000H-01FFFFH	16KB	Top Block
1	0	1	0	X	1	018000H-01FFFFH	32KB	Top Block
1	0	1	1	0	1	018000H-01FFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block
1	X	1	1	1	0 to 1	000000H-01FFFFH	128KB	ALL

Table1.3. GD25Q512 Protected area size

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
0	X	X	0	0	NONE	NONE	NONE	NONE
0	X	X	0	1	0	000000H-00FFFFH	64KB	ALL
0	X	X	1	X	0	000000H-00FFFFH	64KB	ALL
1	X	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	0	00F000H-00FFFFH	4KB	Top Block
1	0	0	1	0	0	00E000H-00FFFFH	8KB	Top Block
1	0	0	1	1	0	00C000H-00FFFFH	16KB	Top Block
1	0	1	0	X	0	008000H-00FFFFH	32KB	Top Block
1	0	1	1	0	0	008000H-00FFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block
1	X	1	1	1	0	000000H-00FFFFH	64KB	ALL

Status Register

S15-S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Reserved	QE	SRP1	SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, only if the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are 0.

SRP1, SRP0 bits.

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	#WP	Status Register	Description
0	0	X	Software Protected	WP# pin has no control. The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	When WP# pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When WP# pin is high the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and can not be written to again until the next Power-Down, Power-Up cycle.(2)
1	1	X	One Time Program(1)	Status Register is permanently protected and can not be written to.

NOTE:

When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground)

COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Status Register	01H	(S7-S0)	(S15-S8)				
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	dummy(5)	(D7-D0)(3)			(continuous)
Quad I/O Word Fast Read(7)	E7H	A23-A0 M7-M0(4)	dummy(6)	(D7-D0)(3)			(continuous)
Continuous Read Reset	FFH						
Page Program	02 H	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32K)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64K)(8)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60 H						
Program/Erase Suspend	75H						
Program/Erase Resume	7AH						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)		(continuous)
Release From Deep Power-Down	ABH						

Manufacturer/ Device ID	90H	dummy	dummy	00H	(M7-M0)	(ID7-ID0)	(continuous)
High Performance Mode	A3H	dummy	dummy	dummy			
Read Identification	9FH	(M7-M0)	(ID15-ID8)	(ID7-ID0)			(continuous)

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

   IO0 = (D4, D0, …..)

   IO1 = (D5, D1, …..)

   IO2 = (D6, D2, …..)

   IO3 = (D7, D3,…..)

4. Quad Input Address

   IO0 = A20, A16, A12, A8, A4, A0, M4, M0

   IO1 = A21, A17, A13, A9, A5, A1, M5, M1

   IO2 = A22, A18, A14, A10, A6, A2, M6, M2

   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Fast Read Quad I/O Data

   IO0 = (x, x, x, x, D4, D0,…)

   IO1 = (x, x, x, x, D5, D1,…)

   IO2 = (x, x, x, x, D6, D2,…)

   IO3 = (x, x, x, x, D7, D3,…)

6. Fast Word Read Quad I/O Data

   IO0 = (x, x, D4, D0,…)

   IO1 = (x, x, D5, D1,…)

   IO2 = (x, x, D6, D2,…)

   IO3 = (x, x, D7, D3,…)

7. Fast Word Read Quad I/O Data: the lowest address bit must be 0.

8. The GD25Q512 has no Block Erase (64K) command.

Table of ID Definitions:

GD25Q40

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	C8	40	13
90H	C8		12
ABH			12

GD25Q20

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	C8	40	12
90H	C8		11
ABH			11

GD25Q10

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	C8	40	11
90H	C8		10
ABH			10

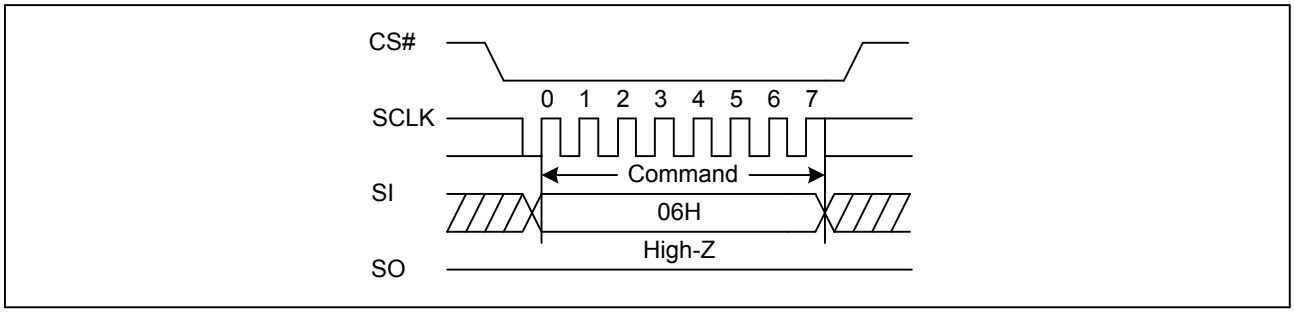
GD25Q512

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	C8	40	10
90H	C8		05
ABH			05

Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

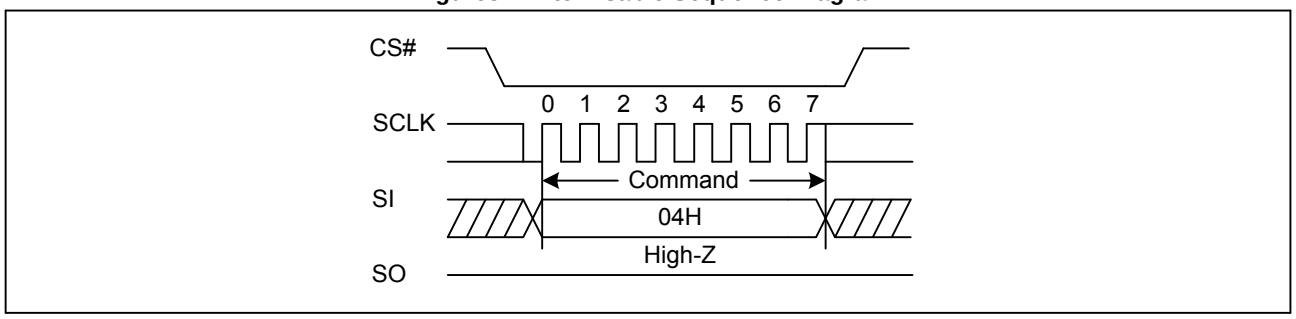
Figure2. Write Enable Sequence Diagram



Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low→Sending the Write Disable command →CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

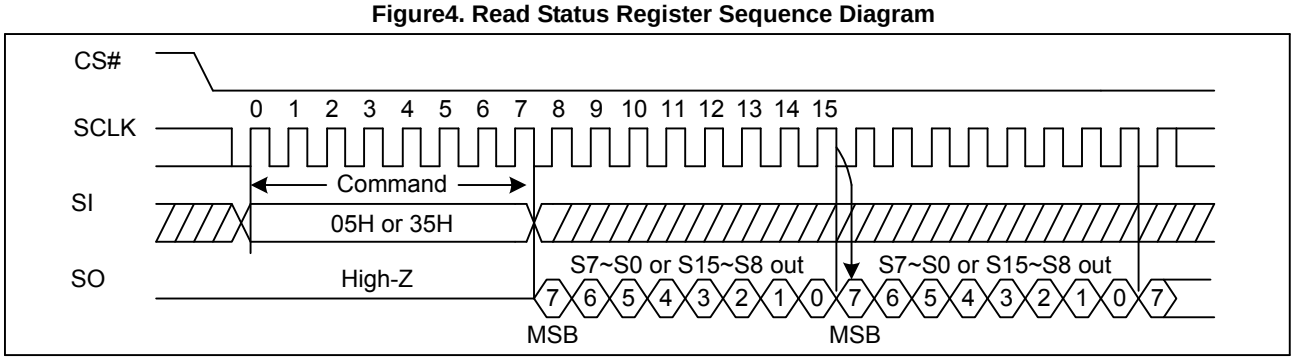
Figure3. Write Disable Sequence Diagram



Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H”, the SO will output Status Register bits S15~S8.

Figure4. Read Status Register Sequence Diagram



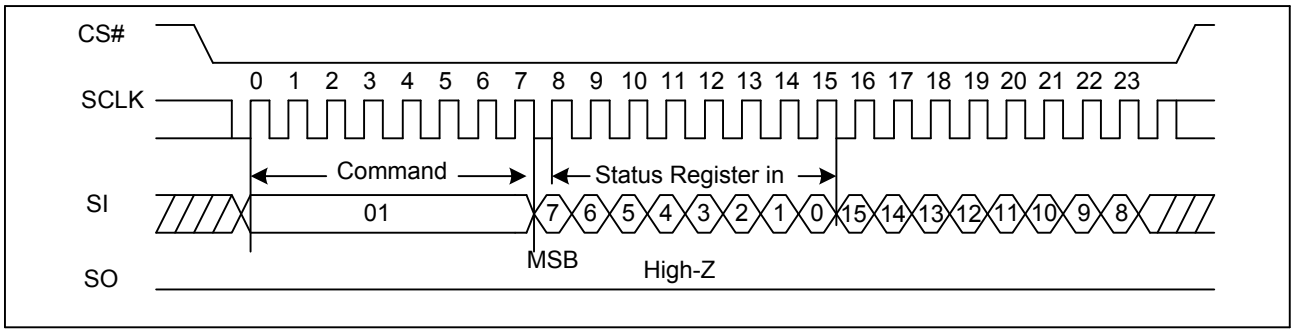
Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15~S10, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the QE and SRP1 bits will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

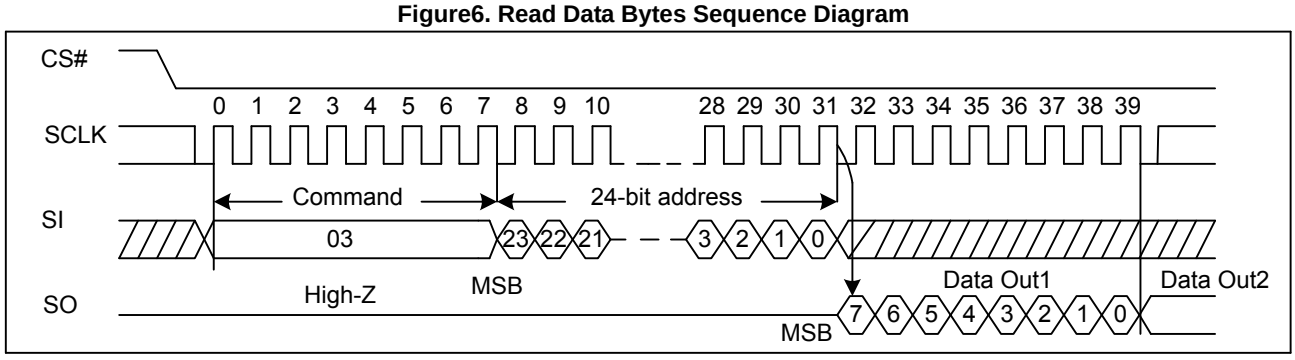
Figure5. Write Status Register Sequence Diagram



Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_R, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

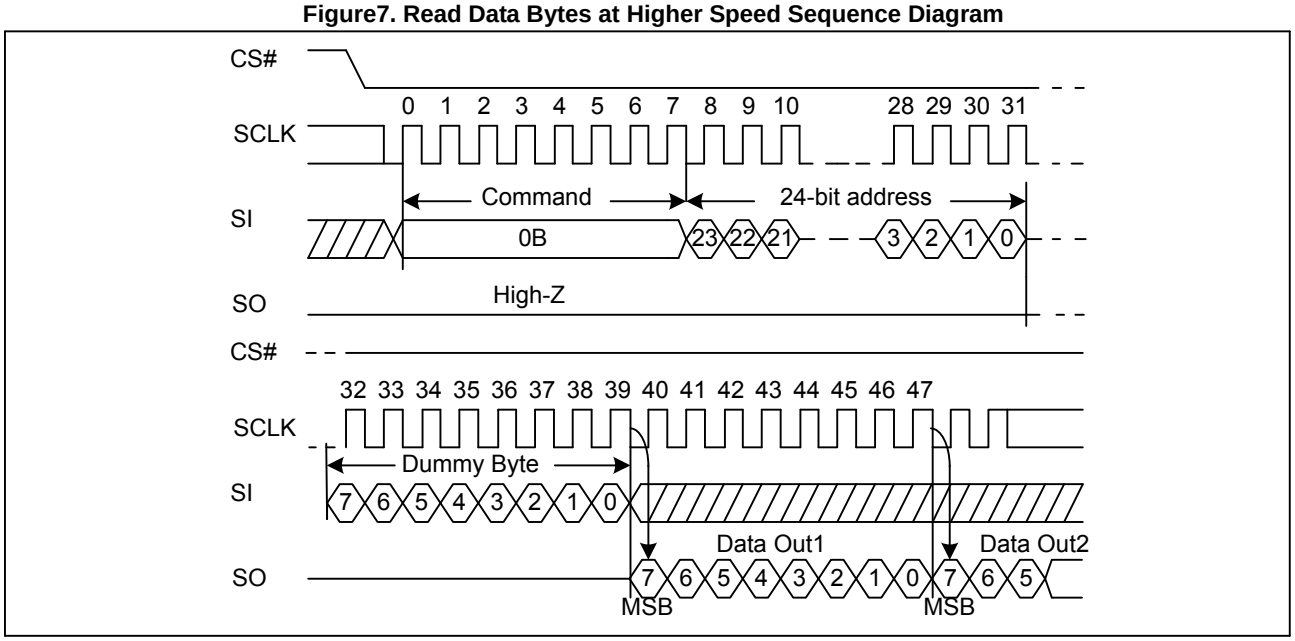
Figure6. Read Data Bytes Sequence Diagram



Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

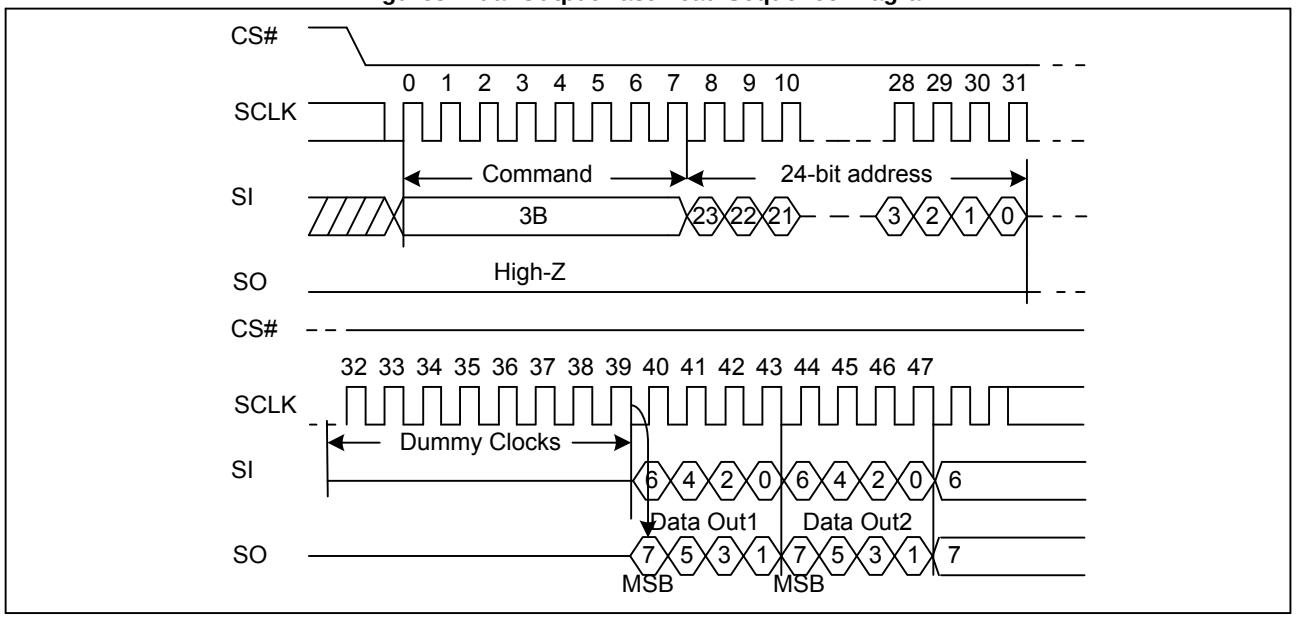
Figure7. Read Data Bytes at Higher Speed Sequence Diagram



Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

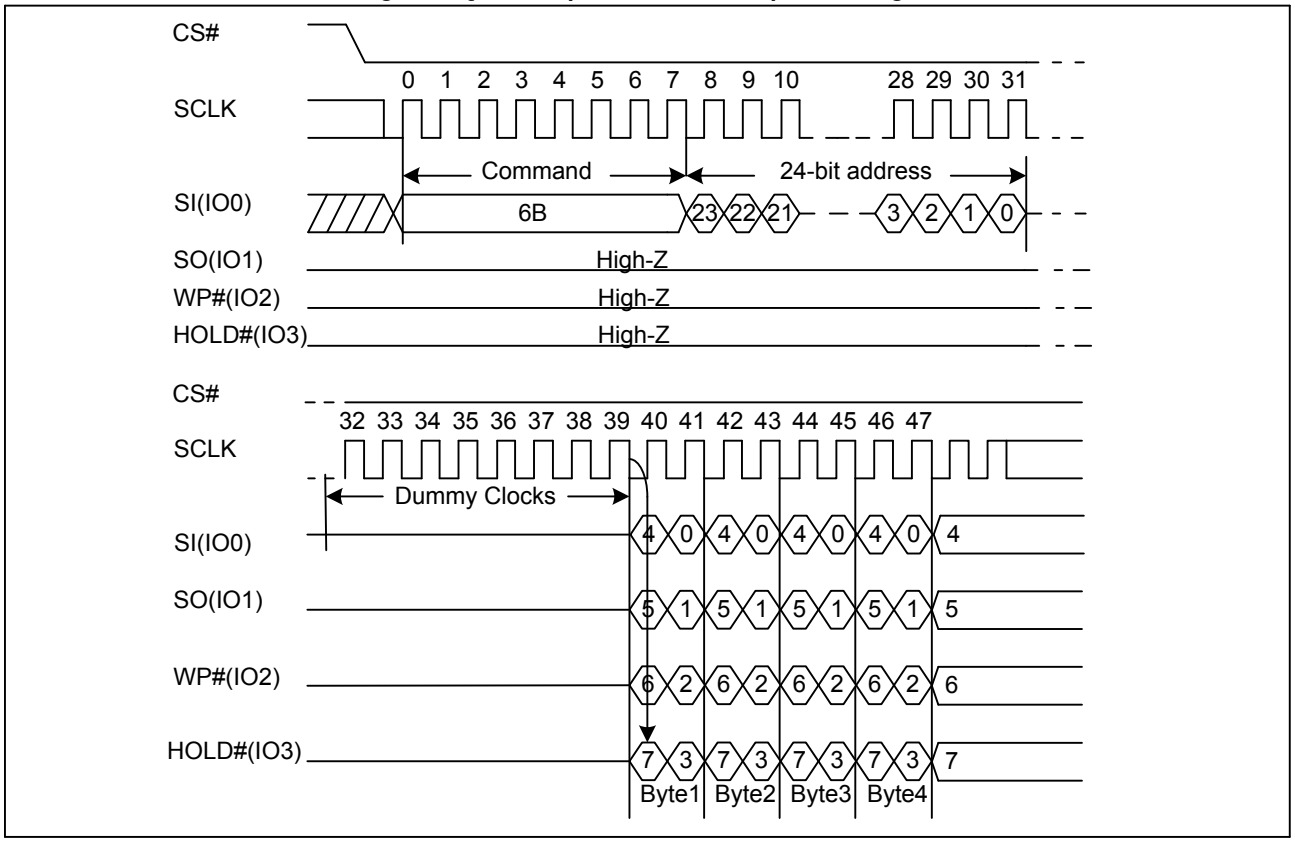
Figure8. Dual Output Fast Read Sequence Diagram



Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure9. Quad Output Fast Read Sequence Diagram



Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. To ensure optimum performance the High Performance Mode (HPM) command (A3H) must be executed once, prior to the Dual I/O Fast Read command.

Dual I/O Fast Read With “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M7-0) =AXH, then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure11. If the “Continuous Read Mode” bits (M7-0) are any value other than AXH, the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M7-0) before issuing normal command.

Figure10. Dual I/O Fast Read Sequence Diagram (M7-0= 0XH or not AXH)

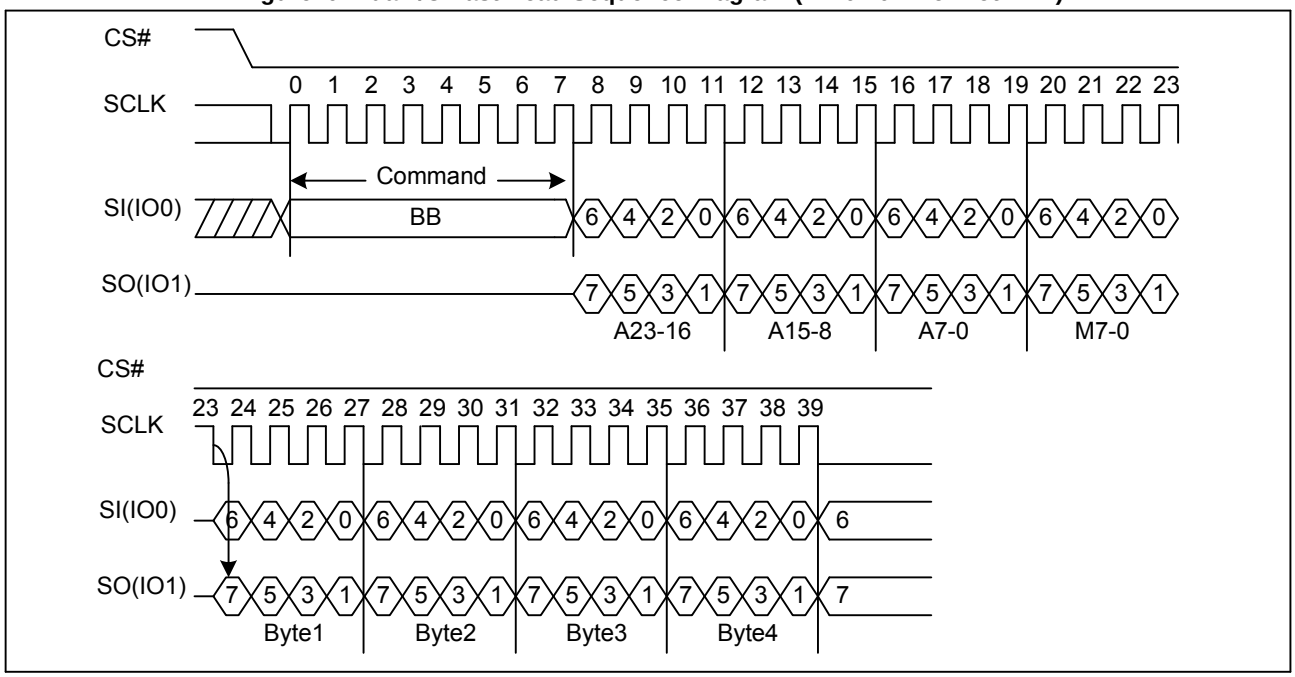
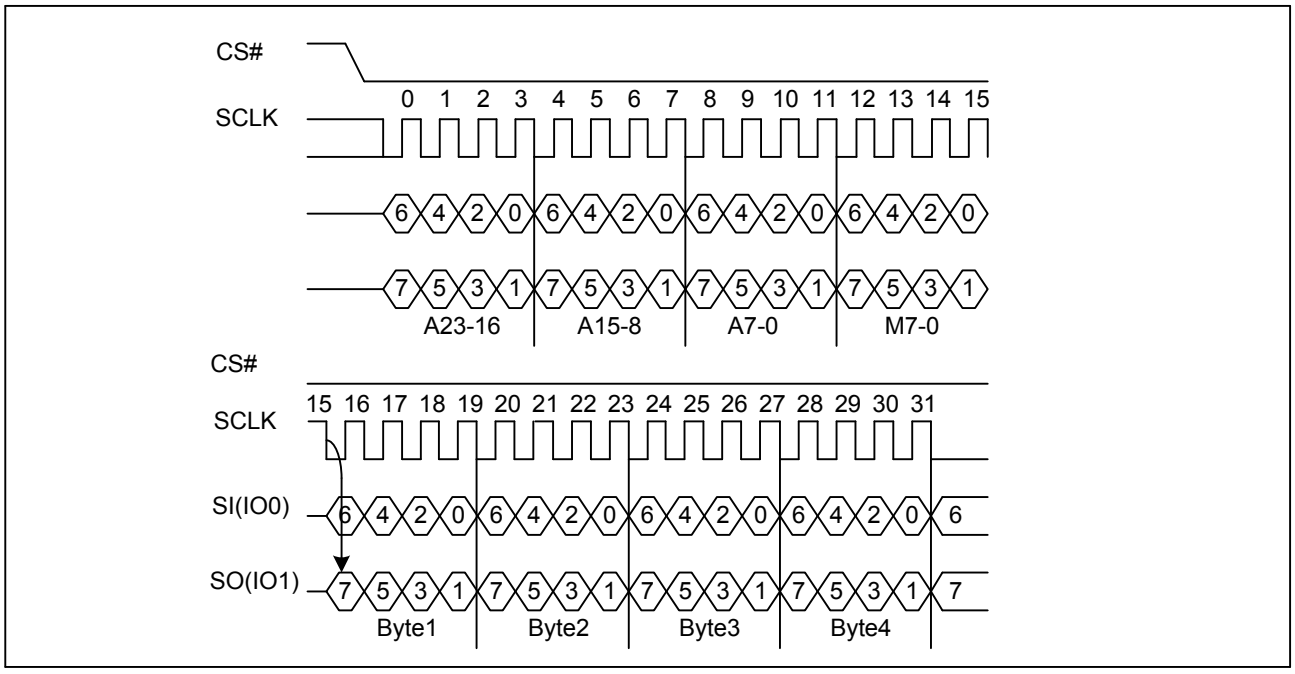


Figure11. Dual I/O Fast Read Sequence Diagram (M7-0= AXH)



Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in followed Figure12. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command. To ensure optimum performance the High Performance Mode (HPM) command (A3H) must be executed once, prior to the Quad I/O Fast Read command.

Quad I/O Fast Read With “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M7-0) =AXH, then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in followed Figure13. If the “Continuous Read Mode” bits (M7-0) are any value other than AXH, the next command requires the first EBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M7-0) before issuing normal command.

Figure12. Quad I/O Fast Read Sequence Diagram (M7-0= 0XH or not AXH)

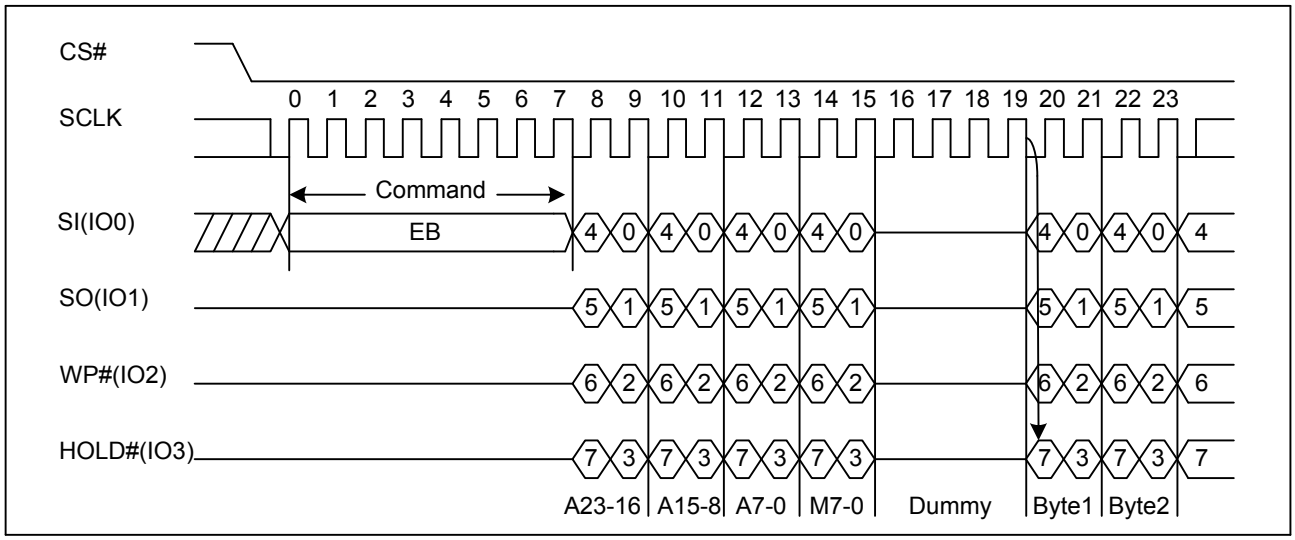
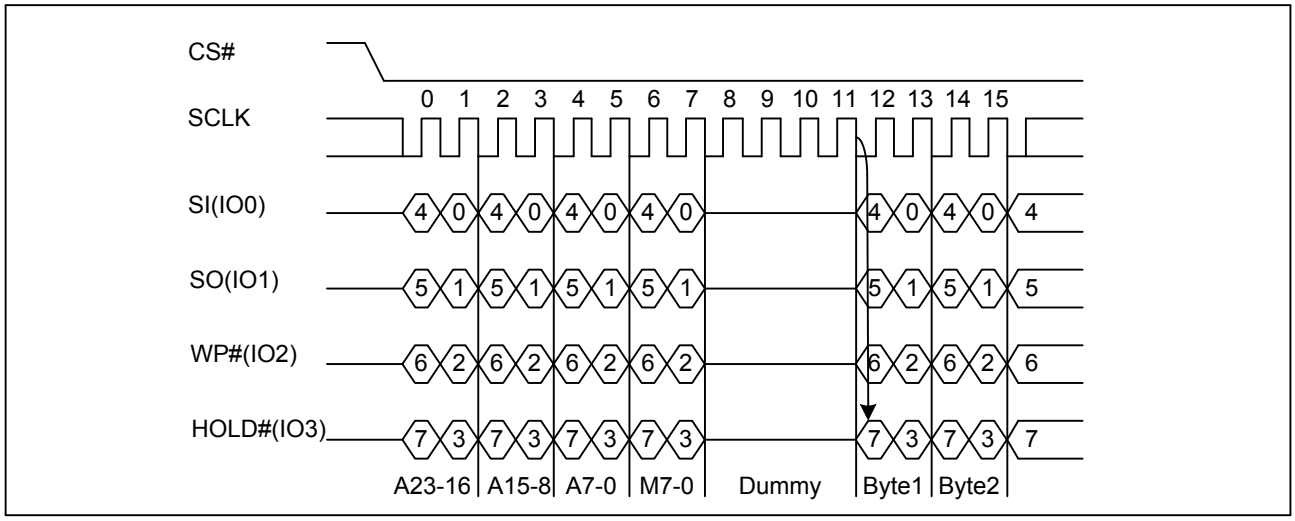


Figure13. Quad I/O Fast Read Sequence Diagram (M7-0= AXH)



Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure14. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command. To ensure optimum performance the High Performance Mode (HPM) command (A3h) must be executed once, prior to the Quad I/O Word Fast Read command.

Quad I/O Word Fast Read With "Continuous Read Mode"

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M7-0) =AXH, then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure15. If the "Continuous Read Mode" bits (M7-0) are any value other than AXH, the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.

Figure14. Quad I/O Word Fast Read Sequence Diagram (M7-0= 0XH or not AXH)

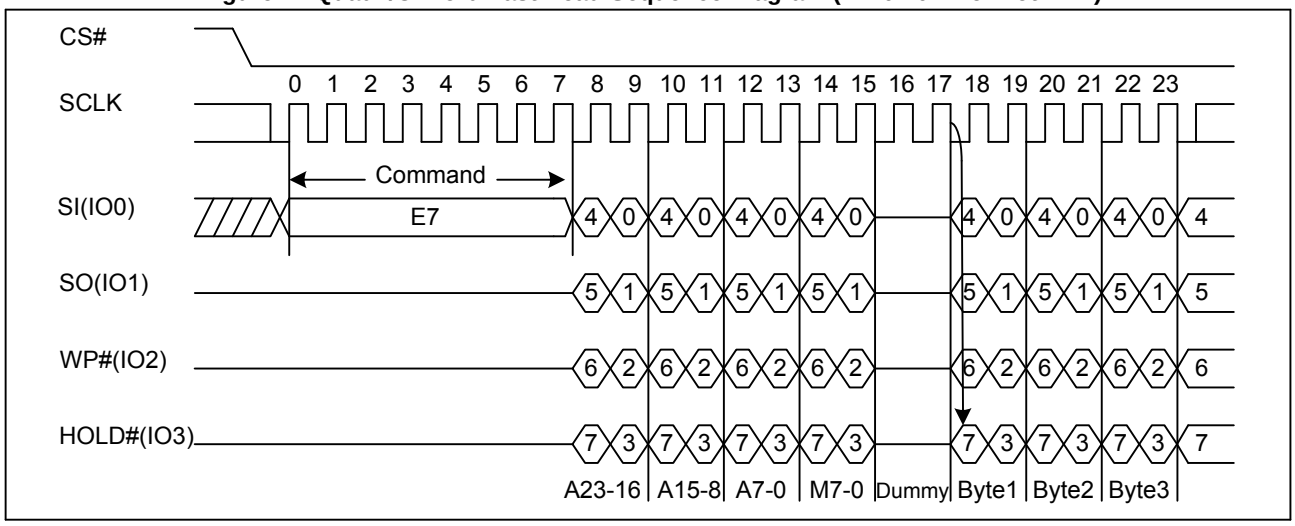
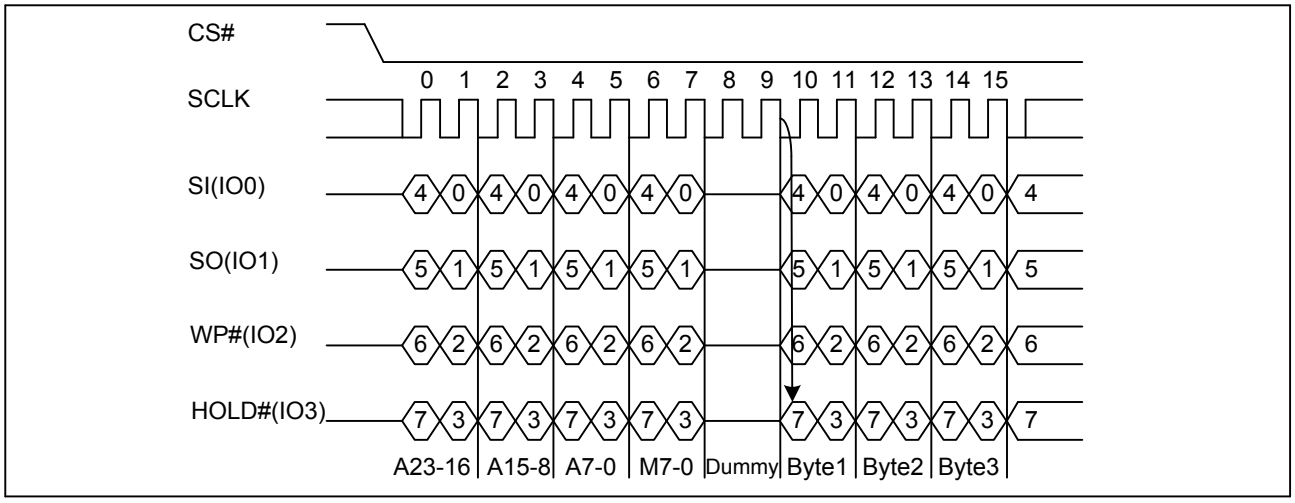


Figure15. Quad I/O Word Fast Read Sequence Diagram (M7-0= AXH)



Page Program (PP) (02H)

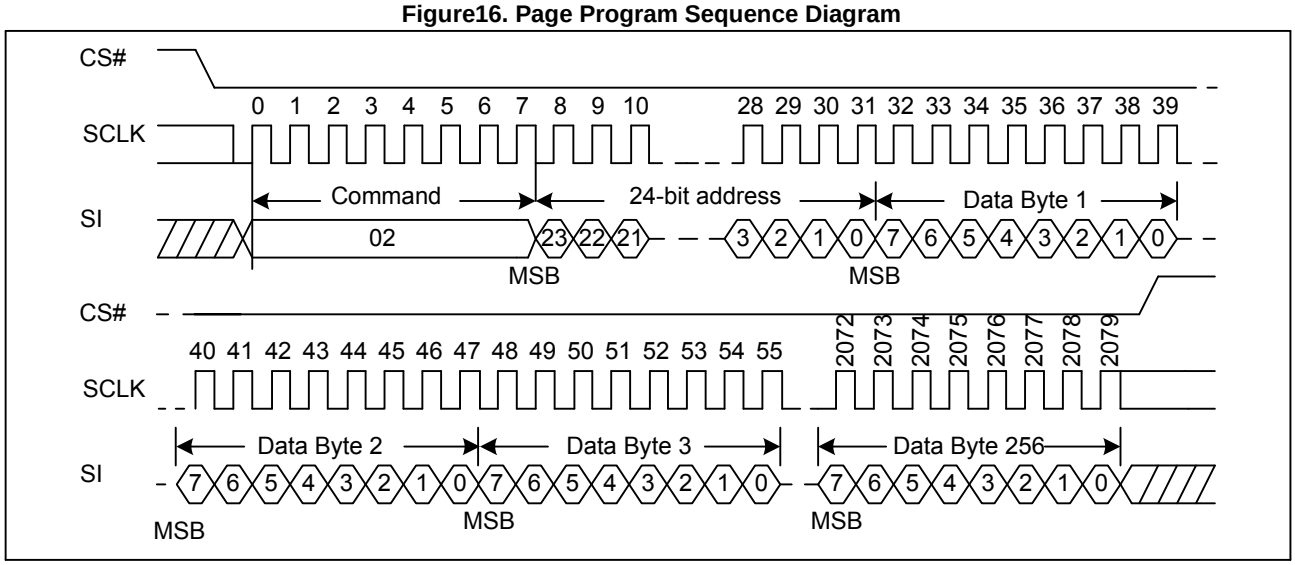
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

Figure16. Page Program Sequence Diagram

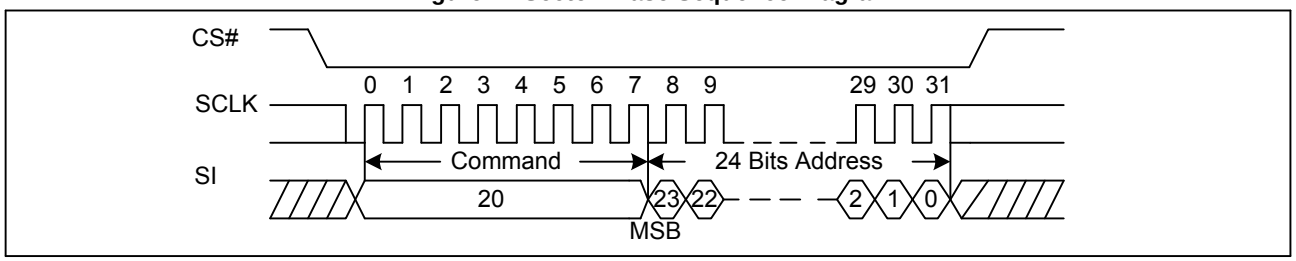


Sector Erase (SE) (20H)

The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure17. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table1.) is not executed.

Figure17. Sector Erase Sequence Diagram

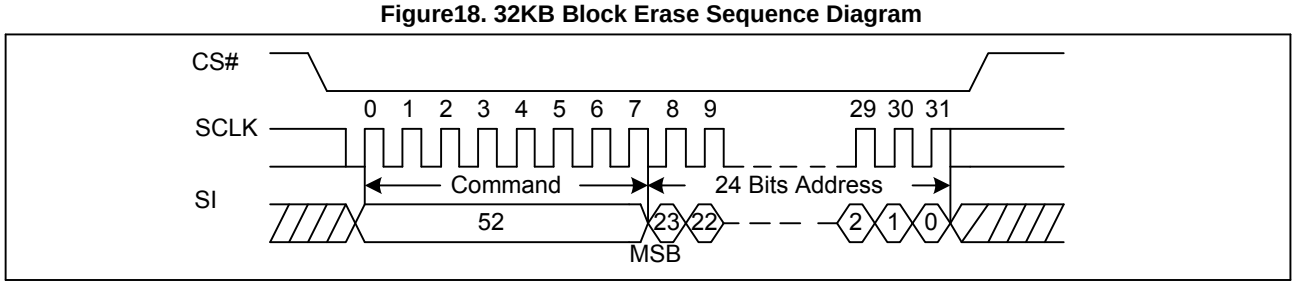


32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure18. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{SE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.) is not executed.

Figure18. 32KB Block Erase Sequence Diagram

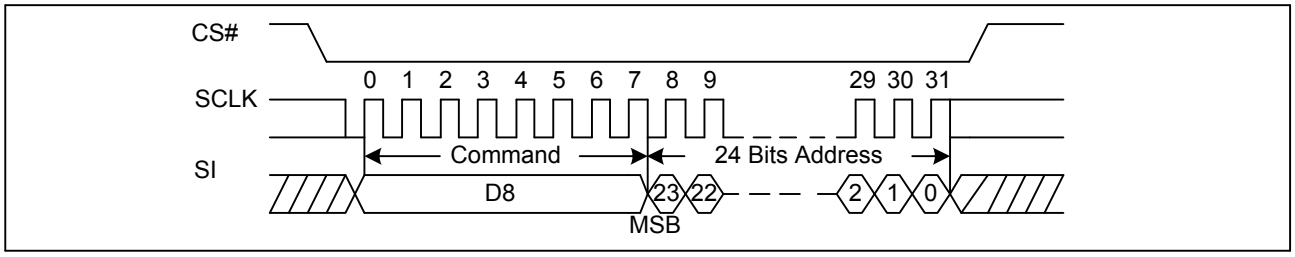


64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure19. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{SE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.) is not executed.

Figure19. 64KB Block Erase Sequence Diagram

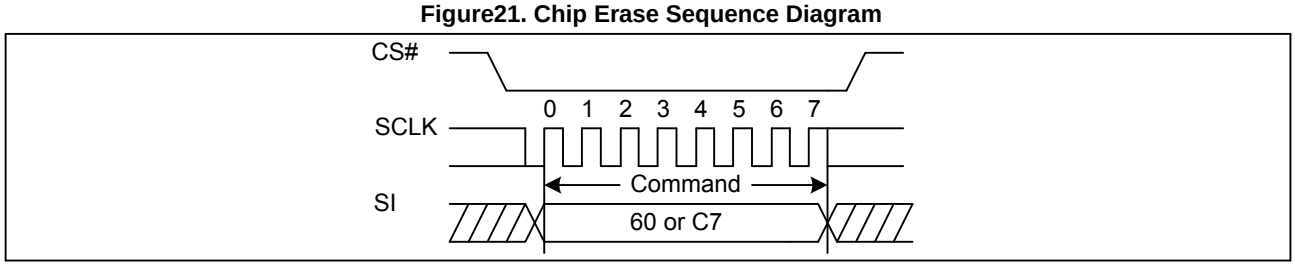


Chip Erase (CE) (60/C7Hex)

The Chip Erase (CE) command is erased the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure21. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure21. Chip Erase Sequence Diagram



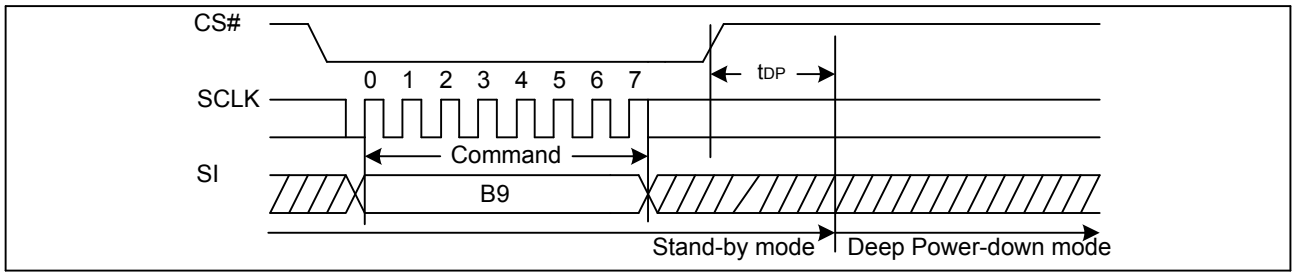
Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. The command sequence is shown in Figure22. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure22. Deep Power-Down Sequence Diagram



Release From Deep Power-Down Or High Performance Mode And Read Device ID (RDI) (ABH)

The Release from Power-Down or High Performance Mode / Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or High Performance Mode or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state or High Performance Mode, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure23. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure23. The Device ID value for the GD25Q16 is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure23, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure23. Release Power-Down Or High Performance Mode Sequence Diagram

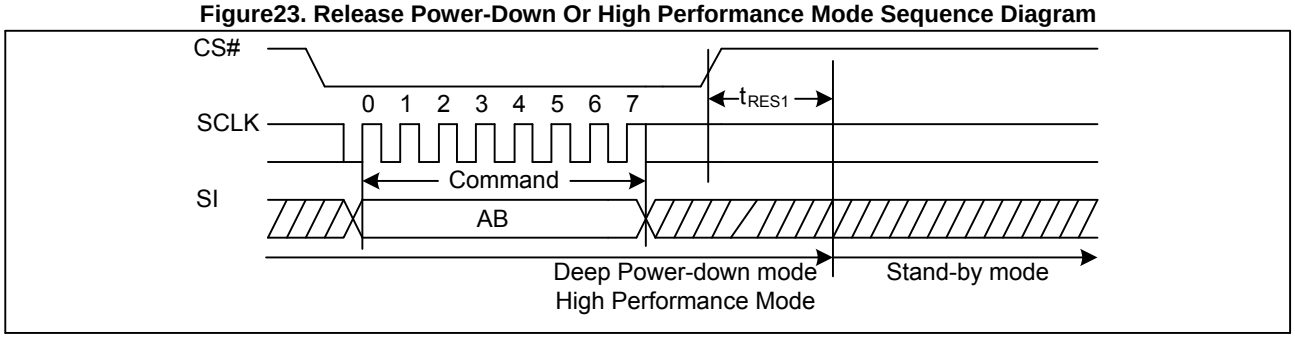
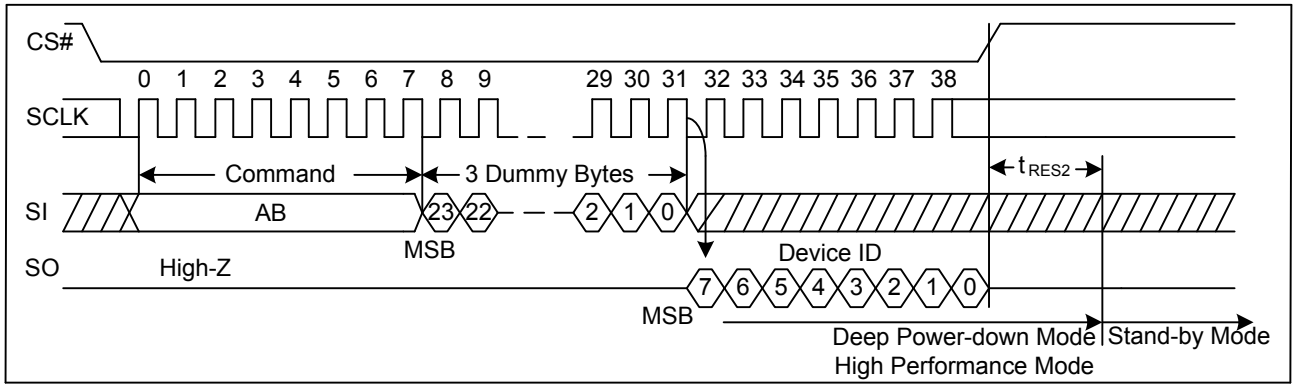


Figure24. Release Power-Down/Read Device ID Sequence Diagram

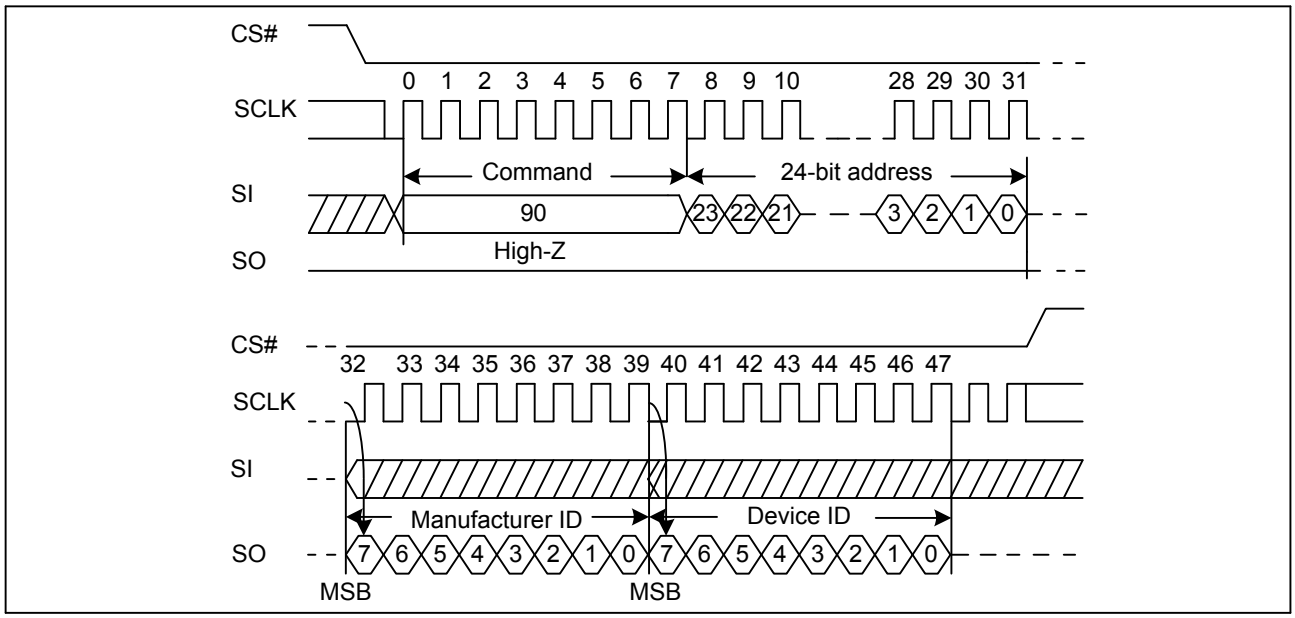


Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure25. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure25. Read Manufacture ID/ Device ID Sequence Diagram

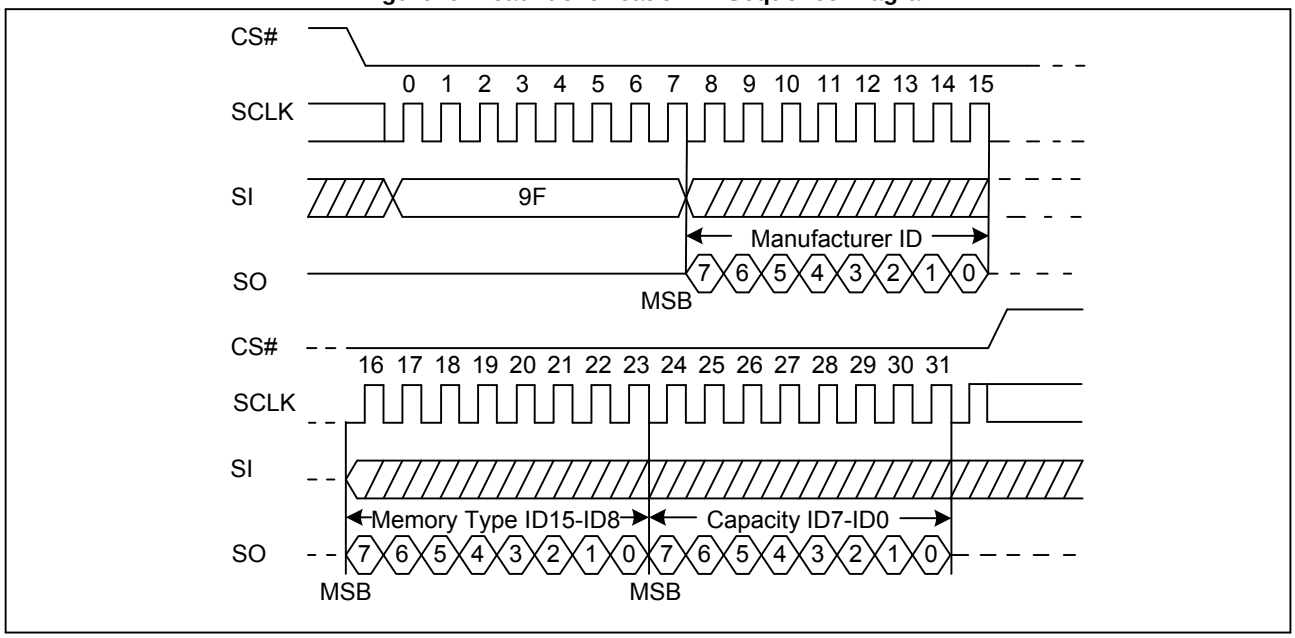


Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure26. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

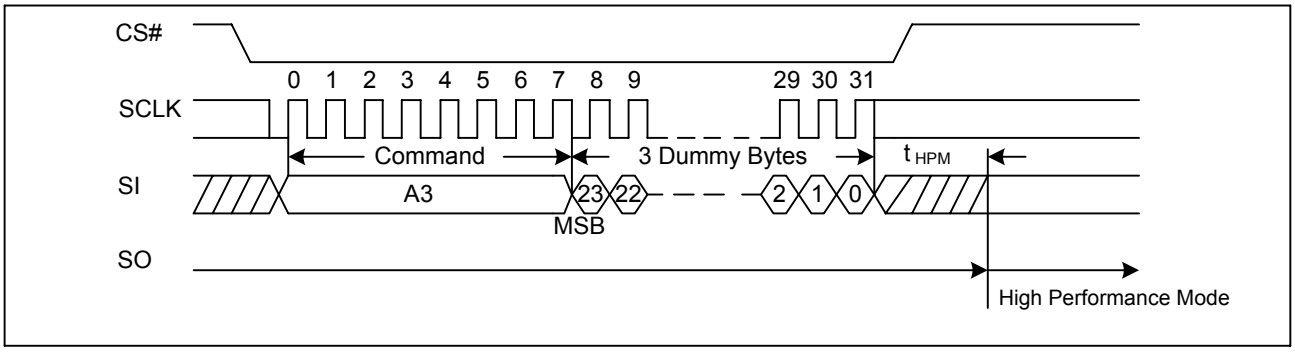
Figure26. Read Identification ID Sequence Diagram



High Performance Mode (HPM) (A3H)

The High Performance Mode (HPM) command must be executed prior to Dual or Quad I/O commands when operating at high frequencies (see f_R and f_C in AC Electrical Characteristics). This command allows pre-charging of internal charge pumps so the voltages required for accessing the flash memory array are readily available. The command sequence: CS# goes low→Sending A3H command→ Sending 3-dummy byte→CS# goes high. See Figure27. After the HPM command is executed, the device will maintain a slightly higher standby current (Icc8) than standard SPI operation. The Release from Power-Down or HPM command (ABH) can be used to return to standard SPI standby current (Icc1). In addition, Write Enable command (06H) and Power-Down command (B9H) will also release the device from HPM mode back to standard SPI standby state.

Figure27. High Performance Mode Sequence Diagram

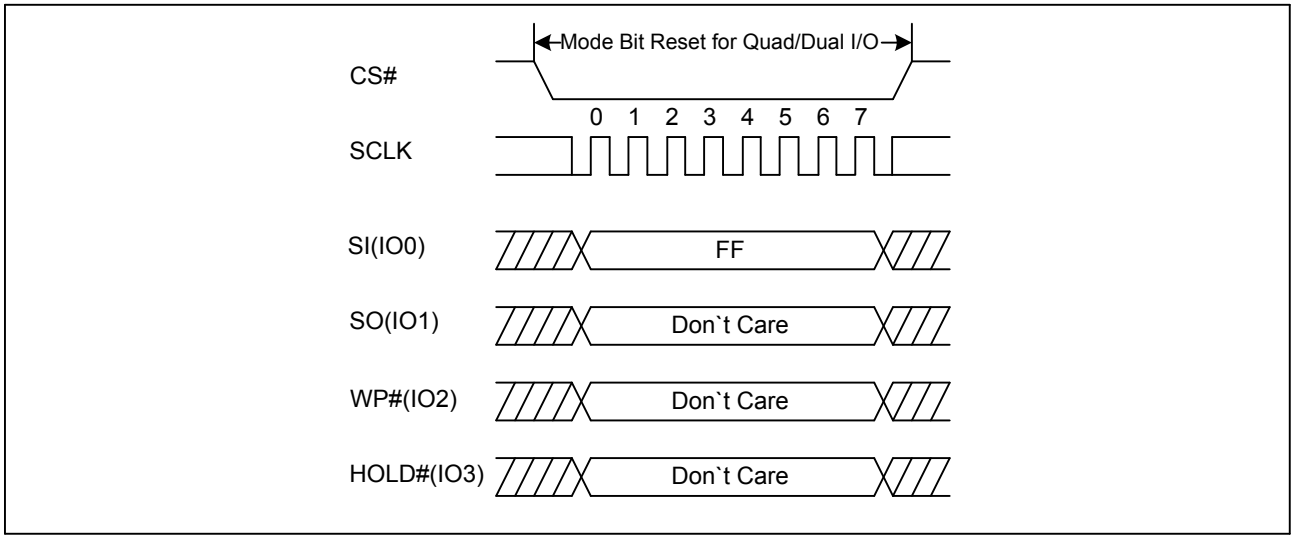


Continuous Read Mode Reset (CRMR) (FFH)

The Dual/Quad I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code.

If the system controller is reset during operation it will likely send a standard SPI command, such as Read ID (9FH) or Fast Read (0BH), to the device. Because the GD25Q40/20/10/512 has no hardware reset pin, so if Continuous Read Mode bits are set to “AXH”, the GD25Q40/20/10/512 will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the “AXH” state and allow standard SPI command to be recognized. The command sequence is show in Figure28.

Figure28. Continuous Read Mode Reset Sequence Diagram

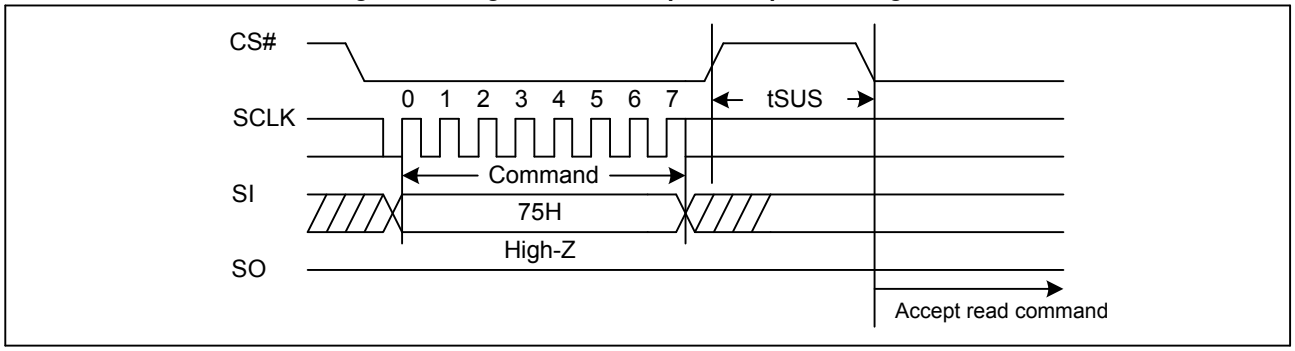


Program/Erase Suspend (PES) (75H)

The Erase/Program Suspend instruction “75H”, allows the system to interrupt a sector/block erase or page program operation and then read data from any other sector or block. The Write Status Register command (01H), Page Program command (02H) and Erase commands (20H, 52H, D8H, C7H, 60H) are not allowed during suspend. Erase/Program Suspend is valid only during the sector/block erase or page program operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

While the Erase/Program suspend cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Erase/Program suspend cycle and becomes a 0 when the cycle is finished and the device is ready to accept read command. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is show in Figure29.

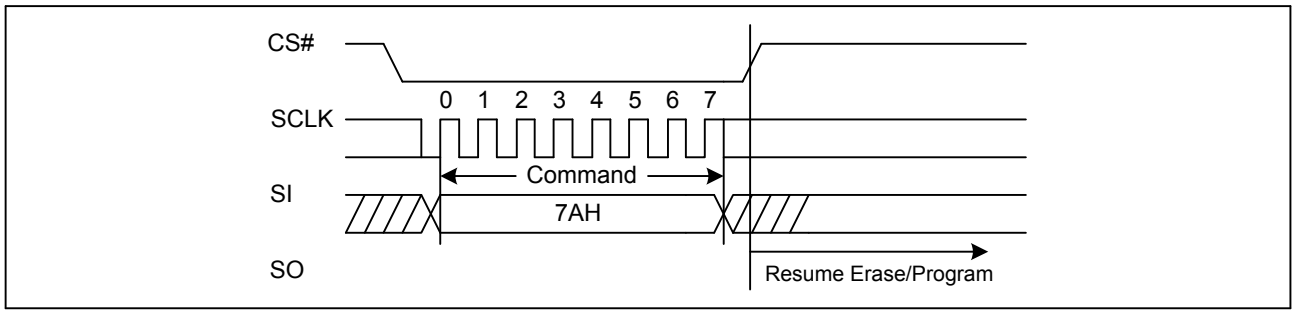
Figure29. Program/Erase Suspend Sequence Diagram



Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the sector/block erase or program operation after a Program/Erase Suspend command. After issued the BUSY bit in the status register will be set to 1 and the sector/block erase or program operation will completed. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is show in Figure30.

Figure30. Program/Erase Resume Sequence Diagram



POWER-ON TIMING

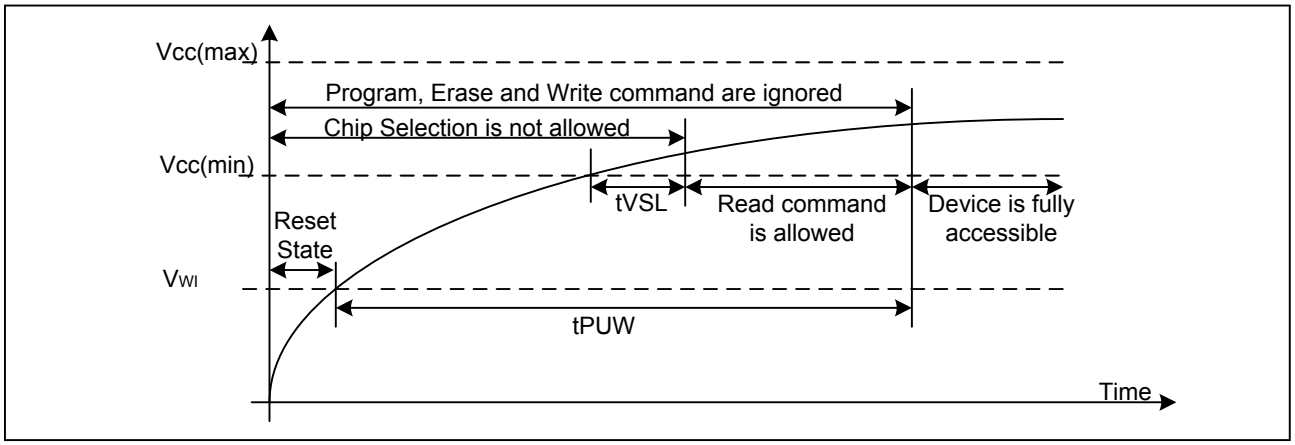


Table3. Power-Up Timing And Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# Low	10		us
tPUW	Time Delay From VCC(min) To Write Instruction	1	10	ms
VWI	Write Inhibit Voltage VCC(min)	1	2.5	V

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

DATA RETENTION AND ENDURANCE

Parameter	Test Condition	Min	Units
Minimum Pattern Data Retention Time	150℃	10	Years
	125℃	20	Years
Erase/Program Endurance	-40 to 85℃	100K	Cycles

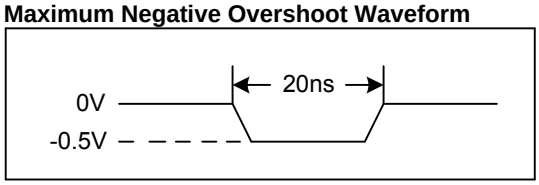
LATCH UP CHARACTERISTICS

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

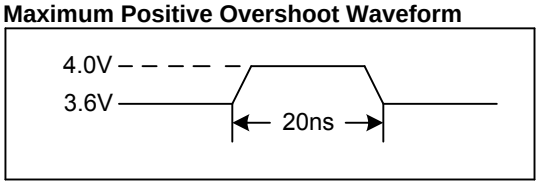
ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-55 to 125	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Maximum Negative Overshoot Waveform



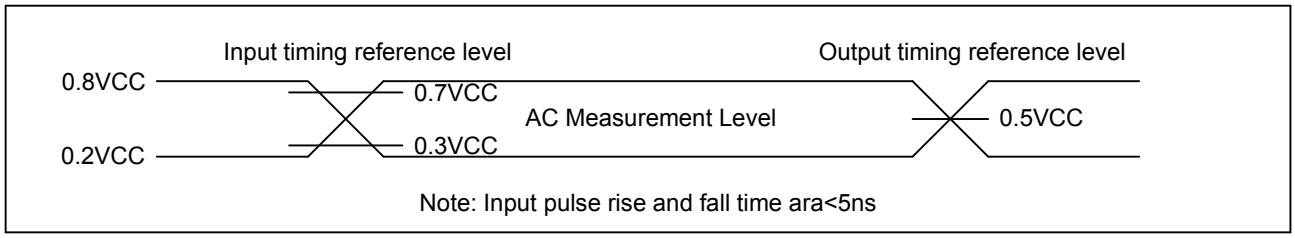
Maximum Positive Overshoot Waveform



CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Tpy	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pause Voltage		0.2VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.3VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure31. Input Test Waveform And Measurement Level



Note: Input pulse rise and fall time ara<5ns

DC CHARACTERISTIC

(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		1	5	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, V_{IN}=VCC or VSS		1	5	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 90MHz, Q=Open(*1,*2,*4 I/O)		15	20	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
I_{CC4}	Operating Current (PP)	CS#=VCC			15	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC			15	mA
I_{CC6}	Operating Current (SE)	CS#=VCC			15	mA
I_{CC7}	Operating Current (BE)	CS#=VCC			15	mA
I_{CC8}	High Performance Current			500	800	uA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

AC CHARACTERISTICS

(T= -40℃~85℃, VCC=2.7~3.6V, C_L=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_C	Serial Clock Frequency For: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR (*1,*2,*4 I/O)	DC.		120	MHz
f_R	Serial Clock Frequency For: Read, RDSR, RDID	DC.		80	MHz
t_{CLH}	Serial Clock High Time	3.5			ns
t_{CLL}	Serial Clock Low Time	3.5			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time（read/write）	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	5			ns
t_{HLCH}	Hold# Low Setup Time (relative to Clock)	5			ns
t_{HHCH}	Hold# High Setup Time (relative to Clock)	5			ns
t_{CHHL}	Hold# High Hold Time (relative to Clock)	5			ns
t_{CHHH}	Hold# Low Hold Time (relative to Clock)	5			ns
t_{HLQZ}	Hold# Low To High-Z Output			6	ns
t_{HHQX}	Hold# Low To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			0.1	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			0.1	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			0.1	μs
t_{HPM}	CS# High To High Performance Mode			0.2	us
t_{SUS}	CS# High To Next Command After Suspend			2	us
t_W	Write Status Register Cycle Time		10	15	ms
t_{PP}	Page Programming Time		0.7	2.4	ms
t_{SE}	Sector Erase Time		150	500	ms
t_{BE}	Block Erase Time(32K\64K)		0.3\0.5	0.75\1.5	s
t_{CE}	Chip Erase Time(GD25Q40\20\10\512)		3\2\1\0.5	7.5\5\2.5\1.5	s

Figure32. Serial Input Timing

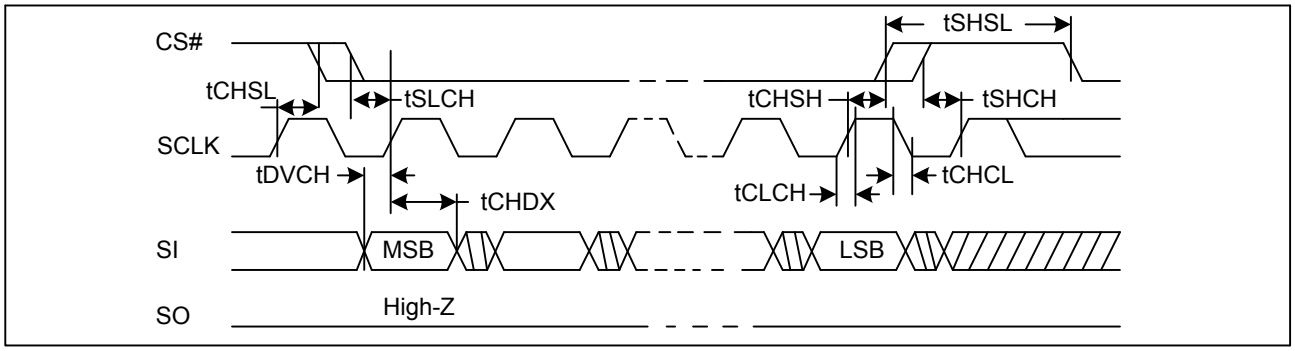


Figure32. Output Timing

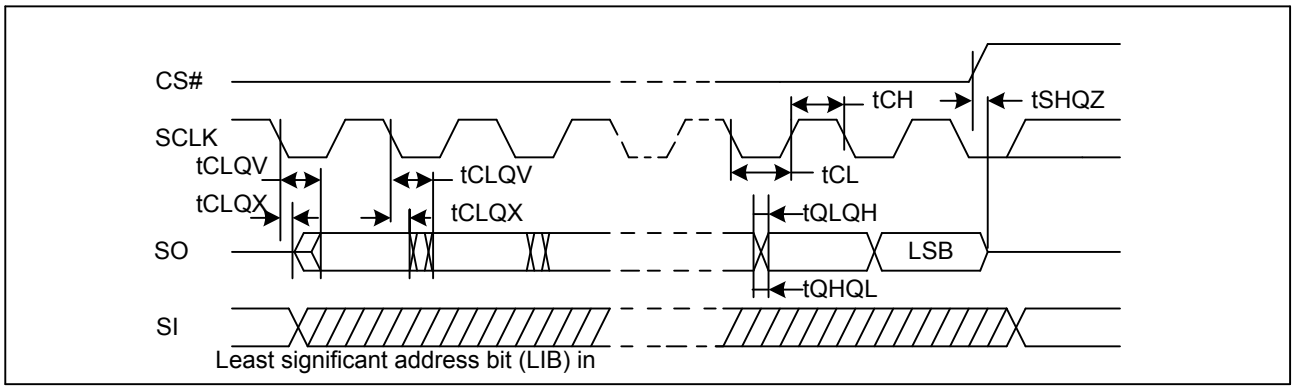
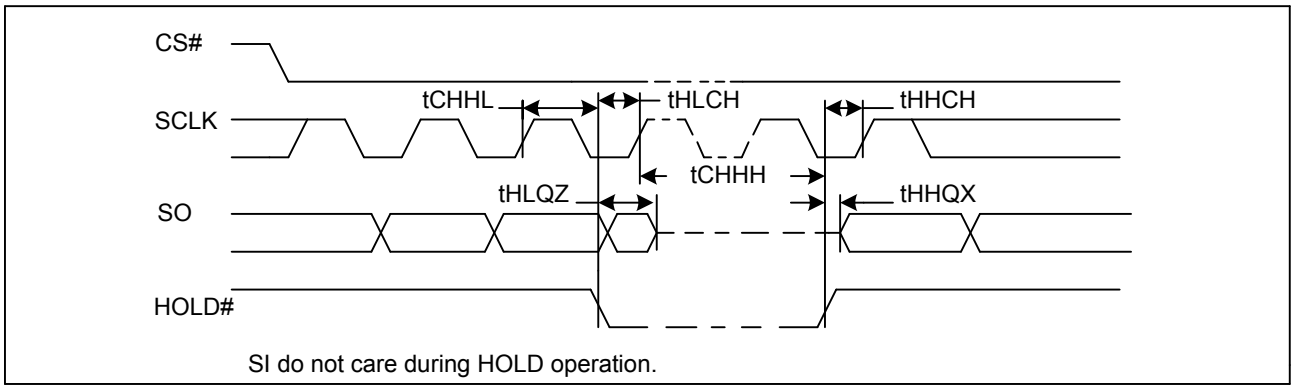
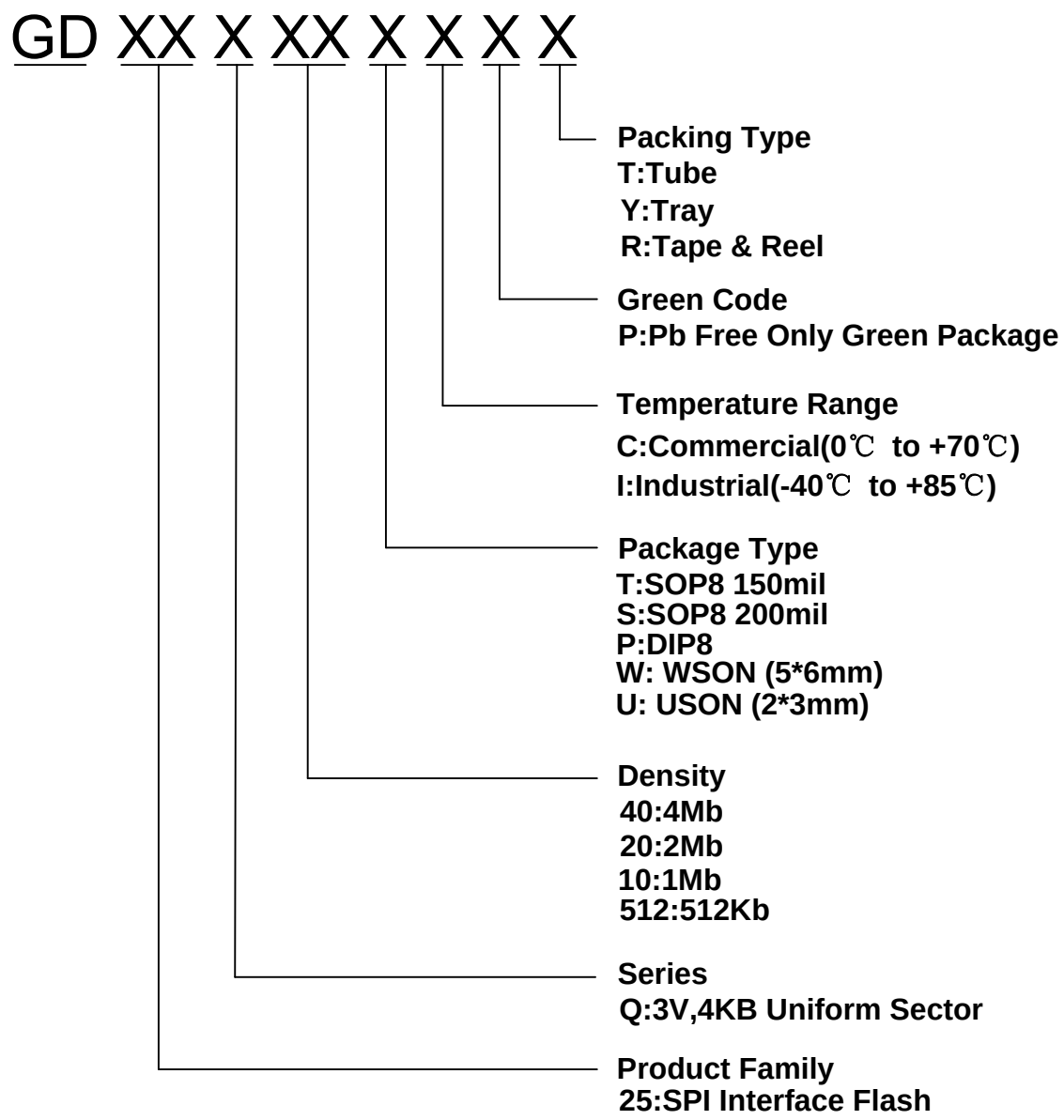


Figure33. Hold Timing



ORDERING INFORMATION

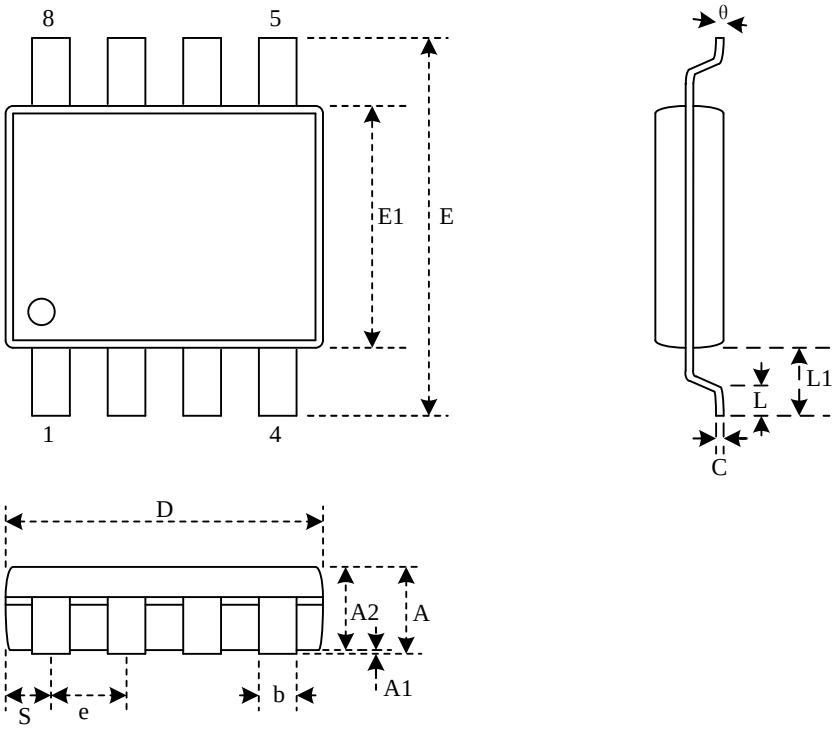


NOTE:

1. Standard bulk shipment is in Tube. Any alternation of packing method (for Tape, Reel and Tray etc.), please advise in advance.

PACKAGE INFORMATION

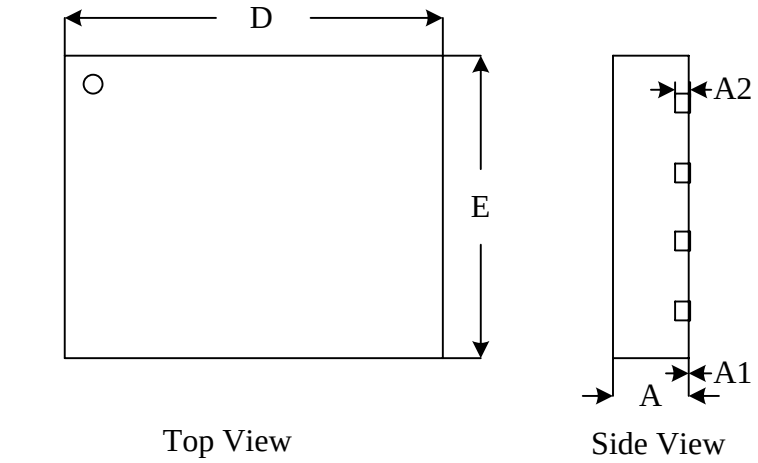
Package SOP8L 150MIL

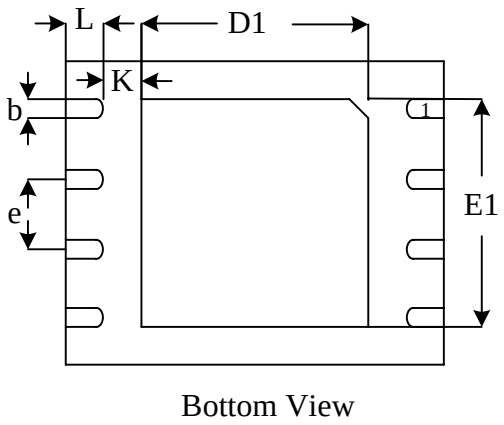


Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min		0.10	1.35	0.36	0.15	4.77	5.80	3.80		0.46	0.85	0.41	0
	Nom		0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5
	Max	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00		0.86	1.25	0.67	8
Inch	Min		0.004	0.053	0.014	0.006	0.188	0.228	0.150		0.018	0.033	0.016	0
	Nom		0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5
	Max	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158		0.034	0.049	0.026	8

Package WSON 8 （5*6mm）

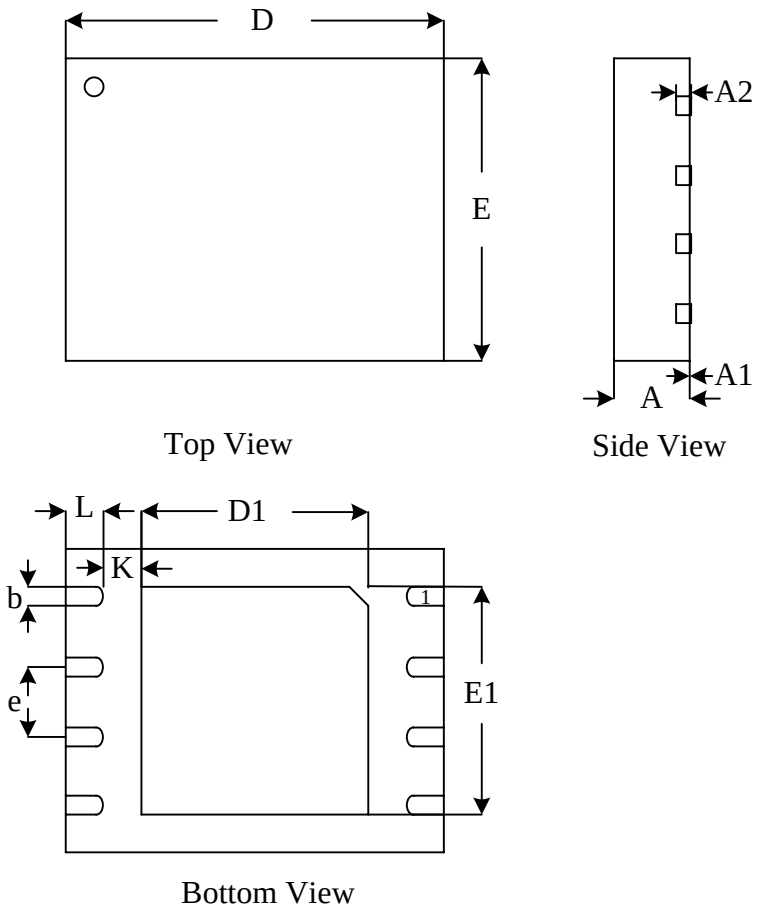




Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	K	L
mm	Min	0.70			0.35	5.90	3.35	4.90	4.25		0.20	0.55
	Nom	0.75		0.20	0.40	6.00	3.40	5.00	4.30	1.27		0.60
	Max	0.80	0.05		0.45	6.10	3.45	5.10	4.35			0.65
Inch	Min	0.028			0.014	0.232	0.132	0.193	0.165		0.008	0.022
	Nom	0.030		0.008	0.016	0.236	0.135	0.197	0.168	0.05		0.024
	Max	0.032	0.002		0.019	0.240	0.137	0.201	0.170			0.027

Package USON 8 （2*3mm）



Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	K	L
mm	Min	0.70		0.18	0.18	2.90		1.90				0.30
	Nom	0.75		0.20	0.25	3.00	1.60	2.00	1.50	0.50		0.40
	Max	0.80	0.05	0.25	0.30	3.10		2.10				0.50
Inch	Min	0.028		0.007	0.007	0.114		0.075				0.012
	Nom	0.030		0.008	0.010	0.118	0.063	0.079	0.059	0.020		0.016
	Max	0.032	0.002	0.010	0.012	0.122		0.083				0.020

REVISION HISTORY

Version No	Description	Date
1.0	Initial Release	Aug.08,2009
1.1	Add t_{HPM} parameter	May.14,2010
1.2	Update AC/DC Characteristics, Add WSON,USON Package	Jun.11,2010