Mini-Circuits

Monolithic Amplifiers

The MAR-cascadable amplifier series is a family of silicon bipolar monolithic integrated circuits fabricated with nitride self-alignment, ion-implantation for precise control of doping and passivation to achieve high reliability. These devices, priced from below one dollar in volume quantity, exhibit excellent unit-to-unit uniformity and are ideally suited as 50-ohm amplifier building blocks. The MAR devices are simple to use if you follow the suggestions given for board layout, proper grounding and steps to minimize parasitics, and correct biasing.

board layout suggestions

In a typical microstrip structure, Fig. 1(a), line impedances are determined by strip width (w), board dielectric material (ε_r), and dielectric thickness (h). Since the impedances of the MAR-units are prematched to operate in a 50 ohm system, microstrip lines should be as close to 50 ohms as possible to realize full specified performance. For various board materials, line width dimensions for a 50-ohm line are given in Fig. 1(b). Operation in systems with characteristic impedances other than 50 ohms is possible with somewhat reduced performance. MAR amplifiers offer very good return loss in a 50-ohm system.

The board material for the microstrip structure should be selected to suit the intended frequency of operation. PTFE woven-glass performs well to frequencies in excess of 2 GHz, is a fairly rugged material that can tolerate substantial rework, and is not particularly sensitive to heat or humidity.

Duroid is the favored material of microwave designers because of its high dielectric consistency and low dielectric dissipation. RT/duroid is a somewhat fragile material which crushes fairly easily; glues do not adhere well to its substrate so thin metallization patterns are subject to lifting if abused with repeated rework. Some versions can also be quite hydroscopic, and can show substantial dielectric shifts with variations in humidity. Because of these factors, care should be taken when working with the material.

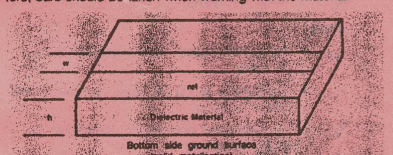


figure 1a

Line Widths for 50 ohm line for various board materials.

Board material	ε	Thick	w/h for 50Ω	w for 50Ω
RT/Duroid 5870[1]	2.3	.015"	2.90	.044"
PTFE-Woven Glass Fiber (Typ.)	2.55	.010"	2.55	.025"
		.031"	2.55	.079"
		.062"	2.55	.158"
Epoxy-Glass (G10)	4.8	.062"	1.75	.108"
Alumina/E10[2]	10.0	.025"	0.95	.024"
		.050"	0.95	.048"

[1] Trademark of Rogers Corp. for its PTFE nonwoven glass PC material. (RT is reinforced teflon and PTFE is polytetrafluoroethylene).
[2] E-10 and Epsilam-10 are trademarks of 3M for its ceramic filled PTFE substrate.

figure 1b

parasitics and grounds

During board layout, care should be taken to minimize all parasitics. Remember that extra lead length equals extra inductance added to the design. This is particularly important if the circuit is to be operated above 1 GHz. Transmission lines should, whenever possible, run flush to the package. This requires that a hole be made in the board so that the MAR-amplifier leads are in the same plane as the transmission line. MAR-amplifiers should be mounted on the etched side of the board to minimize the inductance of feedthrough connections. Abrupt changes in transmission line width also create parasitic effects, called step discontinuities. Although the complete model for such a discontinuity can become quite complicated, the overall effect of the step from an MAR-amplifier lead to a 50 ohm transmission line is typically .05 to .2 nH of extra series inductance. Tapering the transmission lines from 50 ohms down to the amplifier lead width helps minimize this effect. Bends in transmission lines also create parasitic effects and should be avoided when possible; when they must be used, the corners should be chamfered to prevent the bends from acting as extra shunt capacitance. (Reference: K.C. Kupta et all, "Microstrip lines and slot lines," Artech, 1979, p 140-142). The effects of parasitics on gain loss and VSWR, is shown in Table 1.

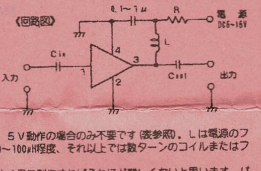
Ground planes should be kept as large and as solid as possible. Return paths for high frequency circulating currents must be kept as short as possible, especially at the emitter leads (MAR ground lead connections). If plated through holes are used as ground returns, they should be placed directly under the ground leads of the MAR and be located as near as possible to the body of the package .050 inches. Any additional path length acts as series inductance, which translates into unwanted emitter resistance at operating frequencies. Gain, power compression, and high frequency rolloff will all be degraded if proper grounding techniques are not used. A gain decrease of more than 1 dB can be expected at 1 GHz for approximately 2nH of lead inductance. Fig. 2 shows good return paths between topside ground connections and the bottom ground plane. The effects of parasitic emitter inductance due to poor RF grounding is shown in Fig. 3, with emitter inductance of zero to 4nH.

table 1 Effects of Parasitics on VSWR and Gain

Freq. MHz	MAR-2, No Parasitics		≈0.9 Parasitic		MAR-2, + Parasitics	
	VSWR	Loss, dB	VSWR	Loss, dB	VSWR	Loss, dB
500	1.09:1	0.0	1.01:1	0.0	1.18:1	.03
1000	1.23:1	.04	1.12:1	.01	1.39:1	.11
1500	1.29:1	.07	1.22:1	.04	1.46:1	.15
2000	1.29:1	.07	1.30:1	.07	1.45:1	.15
2500	1.26:1	.05	1.38:1	.11	1.45:1	.15
3000	1.26:1	.05	1.45:1	.15	1.53:1	.19

figure 2
Methods of realizing minimal length return paths to ground.

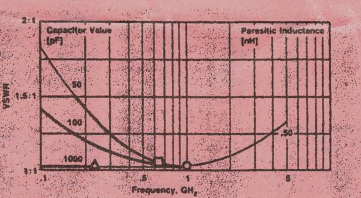
■回路と製作について■
広帯域増幅用に特化したICを使用するため回路構成は非常に簡単です。しかし、取り扱う信号は最高でGHzに及びますので、製作及び使用にあたっては最大限の注意が必要です。
Cin, Coutはカットのための結合コンデンサで1000～2200pF程度、Rはバイアス抵抗で電源電圧により適宜選択します。5V動作の場合のみ不要です（表参照）。Lは電源のフィルタで、おおよそ10MHz以下で10～100μH程度、それ以上では数ターンのコイルまたはフェライトビーズでOKです。
部品点数は少ないので実装図をよく見て製作すればそれほど難しくないと思います。バイアス抵抗（5V以上）や、後述の入力保護のダイオードを取り付ける場合は、パターンをカットして適宜取り付けてください。



DC blocking capacitors are used in both the RF input and output lines to isolate the resistive bias circuits from the source and load resistances. These capacitors will also put limits on the frequency response of the finished amplifier. Low frequency response will be determined by the capacitor's value; it must be high enough to be a reasonable RF "short" at the lowest frequency of operation. High frequency response will be limited to the frequency at which the capacitor's associated parasitic inductance becomes resonant with the blocking capacitor. Operation above the frequency may lead to highly unpredictable circuit behavior. Blocking capacitors with high Qs (Q defined as ratio of capacitive reactance to parasitic resistance) should always be used to minimize insertion losses. Fig. 5 illustrates the variations in VSWR as a function of frequency and value of blocking capacitor.

An RF choke (Dale IM-2 or equivalent) should be used in series with the bias stabilization resistor. Although the choke is not generally needed to keep the RF out of the DC, it is needed to keep the stabilization resistor from appearing in parallel with the load circuit, and thus degrading the output match. A good rule-of-thumb is that the impedance of the choke at the lowest frequency of operation plus the value of the stabilization resistor should be at least 500 ohms. A 10 uH inductor works well as a choke at frequencies as low as 10 MHz; it can be either a molded inductor (for low-cost applications) or a chip inductor (in cases where space is at a premium). At higher frequencies, several turns of wire on a high permeability ferrite bead should be used. If the choke is omitted, expect a gain loss of between 0.5 and 1 dB and a decrease in $P_{1\ dB}$ of as much as 2 dB from the guaranteed performance due to load impedance mismatch.

A large value bypass capacitor (1 uF or so) should be used in conjunction with the choke to present a low impedance path to ground for any signal that does manage to get past the choke. This capacitor should be attached between the supply side of the RF choke and ground.



□ : resonant frequency, .25 nH parasitic inductance
○ : resonant frequency, 0.5 nH parasitic inductance
△ : resonant frequency, 1.0 nH parasitic inductance

figure 5
Effects of DC blocking capacitors on VSWR as a function of frequency, capacitance and parasitic inductance.

S-parameter data

Freq.	S_{11} (Input Return Loss)			S_{21} (Power Gain)		S_{12} (Isolation Out-In)			S_{22} (Output Return Loss)			F
MHz	dB	Mag	Ang	dB	Ang	dB	Mag	Ang	dB	Mag	Ang	
100	-15.92	0.61	-21	33.0	162	-40.00	0.01	38	-4.73	0.58	-24	0.79
500	-8.18	0.39	-77	27.9	109	-27.96	0.04	52	-9.37	0.34	-96	0.75
1000	-11.37	0.27	-113	23.0	80	-24.44	0.06	51	-13.56	0.21	-147	0.89
1500	-11.70	0.26	-139	19.4	62	-21.94	0.08	46	-14.89	0.18	174	0.96
2000	-10.46	0.30	-155	16.9	47	-20.00	0.10	41	-15.39	0.17	153	0.97
2500	-9.63	0.33	-180	14.8	32	-18.42	0.12	32	-14.42	0.19	127	1.01
3000	-8.87	0.36	167	12.9	20	-17.72	0.13	27	-17.08	0.14	111	1.07
3500	-7.54	0.42	153	11.4	6	-17.08	0.14	21	-17.72	0.13	107	1.06
4000	-6.94	0.45	141	9.8	-5	-16.48	0.15	14	-19.17	0.11	106	1.10

single and three-stage layouts

A typical MAR-layout is shown in Fig. 6 using 1/32" PTFE woven-glass board—a reasonable compromise between cost durability, and electrical performance. Note that the transmission lines have no bends and are tapered near the package to minimize step discontinuities. Twelve plated through holes, including two under the emitter leads, provide solid ground planes and minimal emitter parasitics for best high frequency performance. The gaps in the transmission line are appropriate for 50 mil ceramic chip capacitors, which have relatively low associated parasitic inductances—typically about 0.5 nH. Mini-Circuits offers a wide variety of values. The DC pad arrangement requires that a bias stabilization resistor be used, but makes the use of an RF choke optional. If the choke is not used, the stabilization resistor would be connected between the output 50-ohm line and the V_{CC} supply line, and the bypass capacitor would be attached between the V_{CC} line and ground. Spacing is appropriate for 1/4 watt carbon resistors, molded inductors, and 1 uF electrolytic capacitors. The layout has been designed so that Fig. 6 can be repeated for multiple cascaded stages. Overall circuit dimensions are 1" × 1.5" for a single stage, with each additional stage adding one inch to the overall length. A three-stage cascaded design using chip resistors and inductors (R and L in diagram) is shown in Fig. 7.

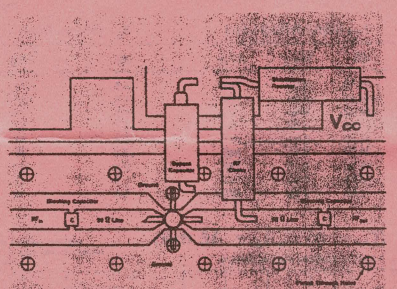


figure 6

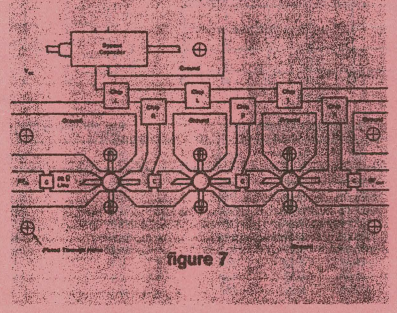


figure 7

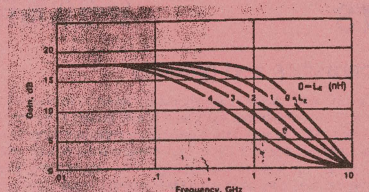


figure 3
Gain vs. frequency as a function of emitter inductance (L_E) for the MAR-1.

for 75-ohm systems

When an ideal 50-ohm unit is used in a 75-ohm system, return loss will drop to 14 dB (VSWR 1.5:1) and mismatch loss will be 0.18 dB at each port. In practice, the return loss change may be higher due to finite isolation. Table 2 shows the gain and return loss of a MAR-3 amplifier in a 75-ohm test system. Gain is about the same as in the 50 ohm system. Input and output return loss (75 ohm) is better than 9 dB over most of the range. At high frequencies there is some improvement in input return loss probably due to the tuning effect of parasitics.

table 2 75-ohm Gain and Return Loss

Frequency (MHz)	Pin (dBm)	Gain (dB)	RL#IN (dB)	RL#OUT (dB)
.30	−32.99	11.72	− 9.78	−11.61
1.	−33.15	11.62	− 9.72	−11.62
12.	−33.54	11.64	− 9.86	−11.69
102.	−33.88	11.57	− 9.75	−11.67
254.	−34.18	11.45	−10.18	−11.63
495.	−34.59	11.29	−11.06	−11.23
1009.	−35.25	10.85	−16.01	−10.38
1507.	−35.50	9.94	−21.23	− 9.99
2200.	−36.17	8.32	−13.50	− 8.72

proper biasing calculations

In order to deliver full performance, MAR-amplifiers must be biased correctly. The internal resistive networks determine individual transistor operating points; all the user needs to do is present the proper voltage at the DC input terminal. For the purpose of bias stability over temperature, the internal transistors should have their bias supplied through a collector resistor (labeled R_C in Fig. 4). This resistor compensates for increases in device β (beta) with temperature by dropping the transistor's collector voltages whenever they try to draw more collector current. Coupled with this effect is the fact that the collector resistor will itself be changing in value over temperature.

Resistors with positive temperature coefficients such as the common carbon composite (+.0001% per degree C°) do an excellent job of compensating for the temperature drift of the negative coefficient on-chip resistors.

For bias stabilization over a temperature range of −10° to +100°C, a drop of at least 1.5 volts across the collector resistor is necessary. The larger this voltage drop, the more stable the bias will be.

For a fixed bias (constant quiescent current vs. temperature), gain will decrease as temperature increases. A voltage drop of about 2V across the collector resistor allows the bias swing over temperature to compensate for this gain change, yielding best gain flatness over temperature. The effect of bias stabilization resistor R_C on performance over a temperature range is shown in Table 3. Notice that the amplifier may self-destruct at high temperatures if no bias resistor is used.

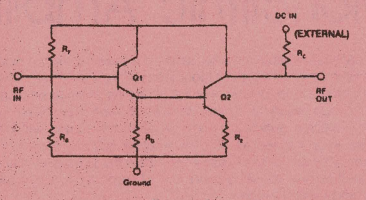


figure 4
General MAR AMP schematic.

table 3 Effects of R_C on performance over temperature.

MAR-1 Operating Voltage = 5.07 V

Voltage Drop, volts	Resistor Value, ohms	Temperature degrees C	Bias Current, mA	Power Gain @ 100 MHz, dB
0	0	−10	9.5	−0.5
		25	18.4	18.8
		100	**	**
1.5	82	−10	14.2	17.0
		25	17.3	18.3
		100	24.1	19.0
2.0	100	−10	16.3	18.5
		25	18.9	18.9
		100	24.6	19.0
7.0	412	−10	16.1	18.3
		25	18.8	18.1
		100	18.3	17.5

** Device destroyed due to excessive current draw.

the value of the bias stabilization resistor R_C is given by:

$$R_C = \frac{V_{cc} - V_d}{I_d} \text{ ohms}$$

where

V_{cc} = the power supply voltage applied to R_C (in volts)

V_d = the voltage at the DC input terminal of the MMIC (in volts)

I_d = the quiescent bias current drawn by the MMIC (in amps)

The dissipation of this resistor is given by:

$$P_{diss} = I_d^2 \times R_C \text{ watts}$$

Table 4 shows the recommended bias resistor values for MAR amplifiers.

table 4 bias resistor values for MAR amplifiers

Amplifier	Bias Current	Bias Voltage	Approximate Bias Resistor (Ohms)				Resistor Dissipation (Watts)
	I_B (mA)	$+V_D$	+5V	+9V	+12V	+15V	$+V_{CC}$=12V
MAR-1	17	~5	—	235	412	588	.12
MAR-2	25	~5	—	160	280	400	.18
MAR-3	35	~5	—	114	200	286	.25
MAR-4	50	~6	—	60	120	180	.30
MAR-6	16	~3.5	98	344	531	719	.14
MAR-7	22	~4	45	227	364	500	.18
MAR-8	36	~8	—	—	111	194	.14

Amplifier Selection Guide

GROUP		MODEL NO.	FREQ. (MHz) f_L	FREQ. (MHz) f_U	GAIN (dB) MIN.	MAX[1] POWER (dBm)	N.F. (dB) TYP.	3rd ORDER I.P. (dBm)	VSWR IN	VSWR OUT	DC POWER V VOLT	DC POWER I (mA)
MONOLITHIC	PIN •	MAR-1	DC	1000	13.0	0	5.0	+15	1.5:1	1.5:1	+5.00	17
	PIN •	MAR-2	DC	2000	8.5	+3	6.5	+18	1.3:1	1.6:1	+5.00	25
	PIN •	MAR-3	DC	2000	8.0	+8	6.0	+23	1.6:1	1.6:1	+5.00	35
	PIN •	MAR-4	DC	1000	7.0	+11	7.0	+27	1.9:1	2.0:1	+5.00	50
	PIN •	MAR-6	DC	2000	9.0	0	2.8	+15	2.0:1	1.8:1	+3.50	16
	PIN •	MAR-7	DC	2000	8.5	+4	5.0	+20	2.0:1	1.5:1	+4.00	22
	PIN •	MAR-8	DC	1000	19.0	+10	3.5	+27	3.1:1	3.1:1	+7.50	36
	PIN •	MAV-1	DC	1000	12.5	+1	5.0	+17	1.4:1	1.4:1	+5.00	17
	PIN •	MAV-2	DC	1500	7.5	+4	7.0	+18	1.6:1	1.6:1	+5.00	25
	PIN •	MAV-3	DC	1500	7.5	+8	6.0	+23	1.6:1	1.6:1	+5.00	35
	PIN •	MAV-4	DC	1000	7.0	+11	7.0	+28	1.8:1	1.8:1	+5.25	50
	PIN •	MAV-11	10	1000	9.0	+16	3.8	+30	2.5:1	2.2:1	+5.60	60

MODEL NO.	•FREQ. MHz f_L	•FREQ. MHz f_U	GAIN, dB Typical (at MHz) 100	500	1000	2000	(Note 4) MIN	MAXIMUM POWER, dBm Output (1dB Comp.)	Input (no damage)	DYNAMIC RANGE NF dB Typ.	IP3 dBm Typ.	VSWR In	VSWR Out	MAXIMUM RATING (25°C) I(mA)	P(mW)	DC POWER at Pin 3 Current (mA)	Volt. Typ.
MAR-1	DC	1000	18.5	17.5	15.5	—	13.0	+ 1.5	+20	5.5	+ 14.0	1.3:1	1.3:1	40	200	17	5.0
MAR-2	DC	2000	12.5	12.3	12.0	11.0	8.5	+ 4.5	+20	6.5	+ 17.0	1.3:1	1.4:1	60	325	25	5.0
MAR-3	DC	2000	12.5	12.2	12.0	10.5	8.0	+ 10.0	+20	6.0	+ 23.0	1.5:1	1.7:1	70	400	35	5.0
MAR-4	DC	1000	8.3	8.2	8.0	—	7.0	+ 12.5	+20	6.5	+ 25.5	1.6:1	2.0:1	85	500	50	5.25
MAR-6	DC	2000	20.0	18.5	16.0	11.0	9.0	+ 2.0	+20	3.0	+ 14.5	1.5:1	1.4:1	50	200	16	3.5
MAR-7	DC	2000	13.5	13.1	12.5	11.0	8.5	+ 5.5	+20	5.0	+ 19.0	1.4:1	1.5:1	60	275	22	4.0
MAR-8	DC	1000	32.5	28.0	22.5	—	19.0	+ 12.5	+20	3.3	+ 27.0	#	#	65	500	36	7.8

MODEL NO.	•FREQ. MHz f_L	•FREQ. MHz f_U	GAIN, dB Typical (at MHz) 100	500	1000	2000	(note 4) MIN.	MAXIMUM POWER, dBm Output (1 dB Comp.)	Input (no damage)	DYNAMIC RANGE NF dB Typ.	IP3 dBm Typ.	VSWR In	VSWR Out	MAXIMUM RATING (25°C) I (mA)	P (mW)	DC POWER at Pin 3 Current (mA)	Volt. Typ.
MAV-1	DC	1000	18.5	17.0	15.0	—	12.5	+ 1.5	+20	5.5	+ 14.0	1.4:1	1.3:1	40	200	17	5.0
MAV-2	DC	1500	12.5	12.0	11.0	10.0	7.5	+ 4.5	+20	6.5	+ 17.0	1.3:1	1.4:1	60	325	25	5.0
MAV-3	DC	1500	12.5	12.0	11.0	10.0	7.5	+ 10.0	+20	6.0	+ 23.0	1.3:1	1.6:1	70	400	35	5.0
MAV-4	DC	1000	8.3	8.0	7.5	—	7.0	+ 11.5	+20	7.0	+ 24.5	1.4:1	1.8:1	85	500	50	5.25
MAV-11	DC	1000	12.7	12.0	10.5	—	9.0	+ 17.5	+20	3.6	+ 30.0	1.5:1	1.7:1	80	550	60	5.5

Monolithic Amplifiers

参考技術資料

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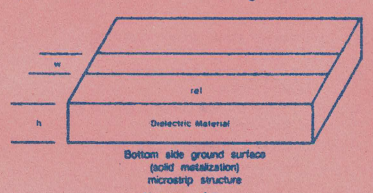

Bottom side ground surface (solid metalization) microstrip structure

figure 1a

Line Widths for 50 ohm line for various board materials.

Board material	ϵ	Thick	w/h for 50Ω	w for 50Ω
RT/Duroid 5870[1]	2.3	.015″	2.90	.044″
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figure 1b

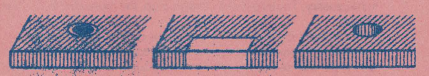
parasitics and grounds

During board layout, care should be taken to minimize all parasitics. Remember that total lead length equals extra inductance added to the design. This is particularly important if the circuit is to be operated above 1 GHz. Transmission lines should, whenever possible, run flush to the package. This requires that a hole be made in the board so that the MAR-amplifier leads are in the same plane as the transmission line. MAR-amplifiers should be mounted on the etched side of the board to minimize the inductance of feedthrough connections. Abrupt changes in transmission line width also create parasitic effects, called step discontinuities. Although the complete model for such a discontinuity can become quite complicated, the overall effect of the step from an MAR-amplifier lead to a 50 ohm transmission line is typically .05 to .2 nH of extra series inductance. Tapering the transmission lines from 50 ohms down to the amplifier lead width helps minimize this effect. Bends in transmission lines also create parasitic effects and should be avoided when possible; when they must be used, the corners should be chamfered to prevent the bends from acting as extra shunt capacitance. (Reference: K.C. Kupta et alt, "Microstrip lines and slot lines," Artech, 1979, p 140-142). The effects of parasitics on gain loss and VSWR, is shown in Table 1.

Ground planes should be kept as large and as solid as possible. Return paths for high frequency circulating currents must be kept as short as possible, especially at the emitter leads (MAR ground lead connections). If plated through holes are used as ground returns, they should be placed directly under the ground leads of the MAR and be located as near as possible to the body of the package .050 inches. Any additional path length acts as series inductance, which translates into unwanted emitter resistance at operating frequencies. Gain, power compression, and high frequency rolloff will all be degraded if proper grounding techniques are not used. A gain decrease of more than 1 dB can be expected at 1 GHz for approximately 2nH of lead inductance. Fig. 2 shows good return paths between topside ground connections and the bottom ground plane. The effects of parasitic emitter inductance due to poor RF grounding is shown in Fig. 3, with emitter inductance of zero to 4nH.

table 1 Effects of Parasitics on VSWR and Gain

Freq. MHz	MAR-2, No Parasitics		≈0.9 nH Parasitics Only		MAR-2, + Parasitics	
	VSWR	Loss, dB	VSWR	Loss, dB	VSWR	Loss, dB
500	1.09:1	0.0	1.01:1	0.0	1.18:1	.03
1000	1.23:1	.04	1.12:1	.01	1.39:1	.11
1500	1.29:1	.07	1.22:1	.04	1.46:1	.15
2000	1.29:1	.07	1.30:1	.07	1.45:1	.15
2500	1.26:1	.05	1.38:1	.11	1.45:1	.15
3000	1.26:1	.05	1.45:1	.15	1.53:1	.19



a. Wire "sewn through" soldered in plate in hole drilled through board. b. "Wrap around" of copper foil (may be used with slit in board). c. Plated through hole (side walls of hole metalized).

figure 2

Methods of realizing minimal length return paths to ground.

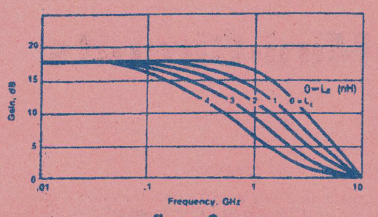


figure 3

Gain vs. frequency as a function of emitter inductance (L_E) for the MAR-1.

for 75-ohm systems

When an ideal 50-ohm unit is used in a 75-ohm system, return loss will drop to 14 dB (VSWR 1.5:1) and mismatch loss will be 0.18 dB at each port. In practice, the return loss change may be higher due to finite isolation. Table 2 shows the gain and return loss of a MAR-3 amplifier in a 75-ohm test system. Gain is about the same as in the 50 ohm system. Input and output return loss (75 ohm) is better than 9 dB over most of the range. At high frequencies there is some improvement in input return loss probably due to the tuning effect of parasitics.

table 2 75-ohm Gain and Return Loss

Frequency (MHz)	Pin (dBm)	Gain (dB)	RL#IN (dB)	RL#OUT (dB)
.30	−32.99	11.72	− 9.78	−11.61
1.	−33.15	11.62	− 9.72	−11.62
12.	−33.54	11.64	− 9.86	−11.69
102.	−33.88	11.57	− 9.75	−11.67
254.	−34.18	11.45	−10.18	−11.63
495.	−34.59	11.29	−11.06	−11.23
1009.	−35.25	10.85	−16.01	−10.38
1507.	−35.50	9.94	−21.23	− 9.99
2200.	−36.17	8.32	−13.50	− 8.72

proper biasing calculations

In order to deliver full performance, MAR-amplifiers must be biased correctly. The internal resistive networks determine individual transistor operating points; all the user needs to do is present the proper voltage at the DC input terminal. For the purpose of bias stability over temperature, the internal transistors should have their bias supplied through a collector resistor (labeled R_C in Fig. 4). This resistor compensates for increases in device β (beta) with temperature by dropping the transistor's collector voltages whenever they try to draw more collector current. Coupled with this effect is the fact that the collector resistor will itself be changing in value over temperature.

Resistors with positive temperature coefficients such as the common carbon composite (+.0001% per degree C°) do an excellent job of compensating for the temperature drift of the negative coefficient on-chip resistors.

For bias stabilization over a temperature range of −10° to +100°C, a drop of at least 1.5 volts across the collector resistor is necessary. The larger this voltage drop, the more stable the bias will be.

For a fixed bias (constant quiescent current vs. temperature), gain will decrease as temperature increases. A voltage drop of about 2V across the collector resistor allows the bias swing over temperature to compensate for this gain change, yielding best gain flatness over temperature. The effect of bias stabilization resistor R_C on performance over a temperature range is shown in Table 3. Notice that the amplifier may self-destruct at high temperatures if no bias resistor is used.

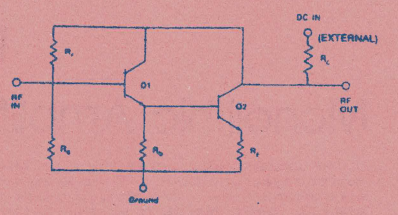


figure 4

General MAR AMP schematic.

table 3 Effects of R_C on performance over temperature.

MAR-1 Operating Voltage = 5.07 V

Voltage Drop, volts	Resistor Value, ohms	Temperature degrees C	Bias Current, mA	Power Gain @100 MHz, dB
0	0	−10	9.5	−0.5
		25	18.4	18.8
		100	**	**
1.5	82	−10	14.2	17.0
		25	17.3	18.3
		100	24.1	19.0
2.0	100	−10	16.3	18.5
		25	18.9	18.9
		100	24.6	19.0
7.0	412	−10	16.1	18.3
		25	18.8	18.1
		100	18.3	17.5

** Device destroyed due to excessive current draw.

the value of the bias stabilization resistor R_C is given by:

$$R_C = \frac{V_{cc} - V_d}{I_d} \text{ ohms}$$

where

V_{cc} = the power supply voltage applied to R_C (in volts)

V_d = the voltage at the DC input terminal of the MMIC (in volts)

I_d = the quiescent bias current drawn by the MMIC (in amps)

The dissipation of this resistor is given by:

$$P_{diss} = I_d^2 \times R_C \text{ watts}$$

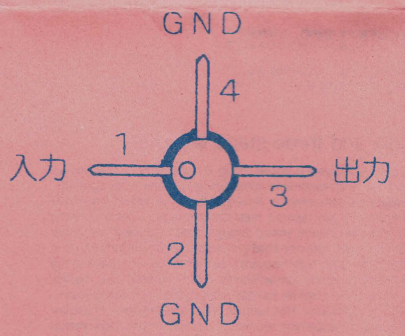
Table 4 shows the recommended bias resistor values for MAR amplifiers.

table 4 bias resistor values for MAR amplifiers

Amplifier	Bias Current	Bias Voltage	Approximate Bias Resistor (Ohms)				Resistor Dissipation (Watts)
	I_B (mA)	$+V_O$	+5V	+9V	+12V	+15V	$+V_{CC}$ = 12V
MAR-1	17	~5	—	235	412	588	.12
MAR-2	25	~5	—	160	280	400	.18
MAR-3	35	~5	—	114	200	286	.25
MAR-4	50	~6	—	60	120	180	.30
MAR-6	16	~3.5	98	344	531	719	.14
MAR-7	22	~4	45	227	364	500	.18
MAR-8	36	~8	—	—	111	194	.14

《ピン配置》

英文記述で文字が小さいため少々大変ですが、
参考になりますので、ぜひご一読ください。

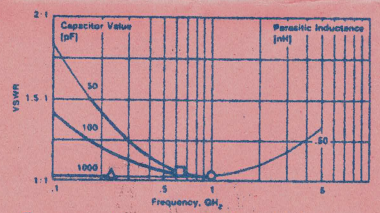


※カラードットのあるピンが
1番(入力)ピン
カラードットは色で区別
{MAR−1：茶色
{MAR−3：オレンジ色

DC blocking capacitors are used in both the RF input and output lines to isolate the resistive bias circuits from the source and load resistances. These capacitors will also put limits on the frequency response of the finished amplifier. Low frequency response will be determined by the capacitor's value; it must be high enough to be a reasonable RF "short" at the lowest frequency of operation. High frequency response will be limited to the frequency at which the capacitor's associated parasitic inductance becomes resonant with the blocking capacitor. Operation above the frequency may lead to highly unpredictable circuit behavior. Blocking capacitors with high Qs (Q defined as ratio of capacitive reactance to parasitic resistance) should always be used to minimize insertion losses. Fig. 5 illustrates the variations in VSWR as a function of frequency and value of blocking capacitor.

An RF choke (Dale IM-2 or equivalent) should be used in series with the bias stabilization resistor. Although the choke is not generally needed to keep the RF out of the DC, it is needed to keep the stabilization resistor from appearing in parallel with the load circuit, and thus degrading the output match. A good rule-of-thumb is that the impedance of the choke at the lowest frequency of operation plus the value of the stabilization resistor should be at least 500 ohms. A 10 uH inductor works well as a choke at frequencies as low as 10 MHz; it can be either a molded inductor (for low-cost applications) or a chip inductor (in cases where space is at a premium). At higher frequencies, several turns of wire on a high permeability ferrite bead should be used. If the choke is omitted, expect a gain loss of between 0.5 and 1 dB and a decrease in $P_{1\ dB}$ of as much as 2 dB from the guaranteed performance due to load impedance mismatch.

A large value bypass capacitor (1 uF or so) should be used in conjunction with the choke to present a low impedance path to ground for any signal that does manage to get past the choke. This capacitor should be attached between the supply side of the RF choke and ground.



□ : resonant frequency, .25 nH parasitic inductance
○ : resonant frequency, 0.5 nH parasitic inductance
△ : resonant frequency, 1.0 nH parasitic inductance

figure 5

Effects of DC blocking capacitors on VSWR as a function of frequency, capacitance and parasitic inductance.

S-parameter data

Freq MHz	S_{11} (Input Return Loss) dB	Mag	Ang	S_{21} (Power Gain) dB	Ang	S_{12} (Isolation Out-In) dB	Mag	Ang	S_{22} (Output Return Loss) dB	Mag	Ang	K
100	−15.92	0.61	24	33.0	162	−40.00	0.01	38	−4.73	0.58	−24	0.79
500	−8.18	0.39	−77	27.8	109	−27.96	0.04	52	−9.37	0.34	−96	0.75
1000	−11.37	0.27	−113	23.0	80	−24.44	0.06	51	−13.56	0.21	−147	0.89
1500	−11.70	0.26	−139	19.4	52	−21.94	0.08	46	−14.89	0.18	174	0.96
2000	−10.46	0.30	155	16.9	47	−20.00	0.10	41	−15.39	0.17	153	0.97
2500	−9.63	0.33	−180	14.8	32	−18.42	0.12	32	−14.42	0.19	127	1.01
3000	−8.87	0.36	167	12.9	20	−17.72	0.13	27	−17.08	0.14	111	1.07
3500	−7.54	0.42	153	11.4	6	−17.08	0.14	21	−17.72	0.13	107	1.06
4000	−6.94	0.45	141	9.8	−5	−16.48	0.15	14	−19.17	0.11	106	1.10

single and three-stage layouts

A typical MAR-layout is shown in Fig. 6 using 1/32″ PTFE woven-glass board—a reasonable compromise between cost durability, and electrical performance. Note that the transmission lines have no bends and are tapered near the package to minimize step discontinuities. Twelve plated through holes, including two under the emitter leads, provide solid ground planes and minimal emitter parasitics for best high frequency performance. The gaps in the transmission line are appropriate for 50 mil ceramic chip capacitors, which have relatively low associated parasitic inductances—typically about 0.5 nH. Mini-Circuits offers a wide variety of values. The DC pad arrangement requires that a bias stabilization resistor be used, but makes the use of an RF choke optional. If the choke is not used, the stabilization resistor would be connected between the output 50-ohm line and the V_{CC} supply line, and the bypass capacitor would be attached between the V_{CC} line and ground. Spacing is appropriate for 1/4 watt carbon resistors, molded inductors, and 1 uF electrolytic capacitors. The layout has been designed so that Fig. 6 can be repeated for multiple cascaded stages. Overall circuit dimensions are 1″ × 1.5″ for a single stage, with each additional stage adding one inch to the overall length. A three-stage cascaded design using chip resistors and inductors (R and L in diagram) is shown in Fig. 7.

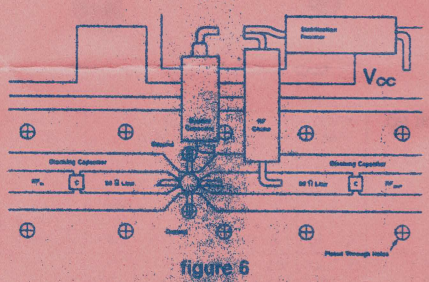


figure 6

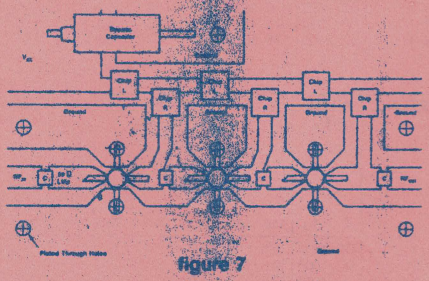
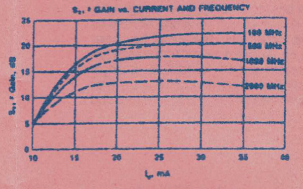
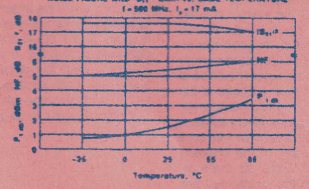
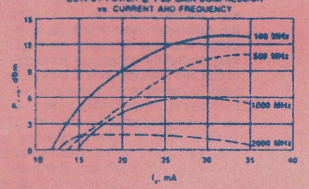


figure 7

MAR-1 (T_A = 25°C, I_d = 17 mA)

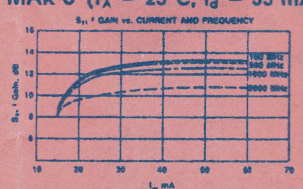


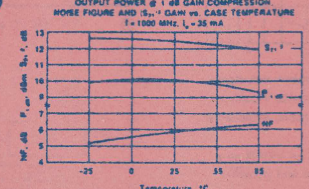


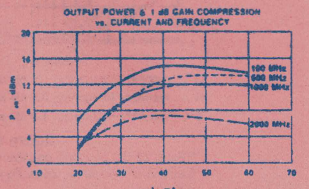


Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Ang	S_{21} (Power Gain) dB	Ang	S_{12} (Isolation Out-In) dB	Mag	Ang	S_{22} (Output Return Loss) dB	Mag	Ang
100	−23.10	0.07	164	18.5	171	−21.94	0.08	4	−23.10	0.07	−14
500	−24.44	0.06	106	17.5	141	−21.94	0.08	15	−23.10	0.07	−68
1000	−24.44	0.06	72	15.5	111	−20.00	0.10	24	−20.92	0.09	−124
1500	−27.96	0.04	59	13.7	87	−17.72	0.13	26	−20.00	0.10	−161
2000	−24.44	0.06	149	12.3	67	−15.92	0.16	21	−15.92	0.16	−177
2500	−20.00	0.10	142	10.6	49	−14.89	0.18	18	−15.92	0.16	155
3000	−18.42	0.12	139	9.3	34	−13.98	0.20	12	−16.48	0.15	144
3500	−13.98	0.20	129	7.9	19	−13.15	0.22	5	−15.92	0.16	135
4000	−11.06	0.28	120	6.6	3	−12.04	0.25	−4	−15.39	0.17	127

MAR-3 (T_A = 25°C, I_d = 35 mA)







Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Ang	S_{21} (Power Gain) dB	Ang	S_{12} (Isolation Out-In) dB	Mag	Ang	S_{22} (Output Return Loss) dB	Mag	Ang
100	−23.10	0.07	172	13.0	174	−18.42	0.12	1	−16.48	0.15	−11
500	−24.44	0.06	156	12.8	152	−18.42	0.12	5	−15.92	0.16	−45
1000	−24.02	0.06	146	12.5	128	−17.72	0.13	10	−14.98	0.18	−88
1500	−27.96	0.04	172	11.8	103	−17.08	0.14	12	−13.56	0.21	−120
2000	−24.44	0.06	173	10.5	83	−14.98	0.18	11	−12.04	0.25	−142
2500	−15.39	0.17	175	10.3	59	−14.42	0.19	5	−11.70	0.26	−173
3000	−12.40	0.24	157	9.1	38	−13.98	0.20	−0	−12.04	0.25	168
3500	−9.90	0.32	140	7.8	21	−13.56	0.21	−6	−12.04	0.25	152
4000	−8.18	0.39	124	6.5	3	−13.15	0.22	−14	−12.04	0.25	138

Mini-Circuits